에이디반도체

TS08N

8-Channel Self Calibration Capacitive Touch Sensor

SPECIFICATION V3.0

1 Specification

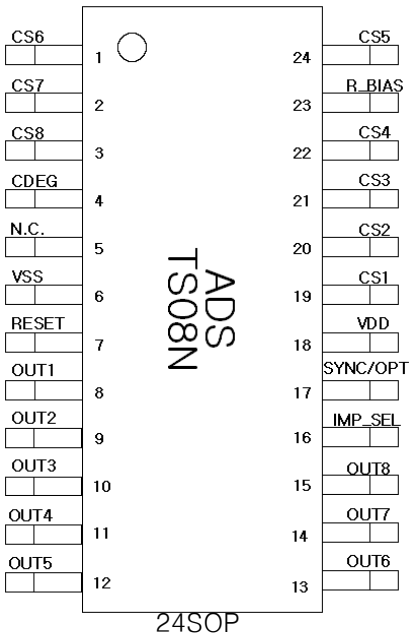
1.1 General Feature

- 8-Channel capacitive sensor with auto sensitivity calibration
- Selectable output operation (single or multi output mode)
- Low current consumption
- Uniformly adjustable 2 step sensitivity
- Sync function for parallel operation
- Adjustable internal frequency with external resister
- Selectable sense line impedance out of scanning
- Open-drain digital output
- Embedded common and normal noise elimination circuit
- RoHS compliant 24SOP and 32QFN package

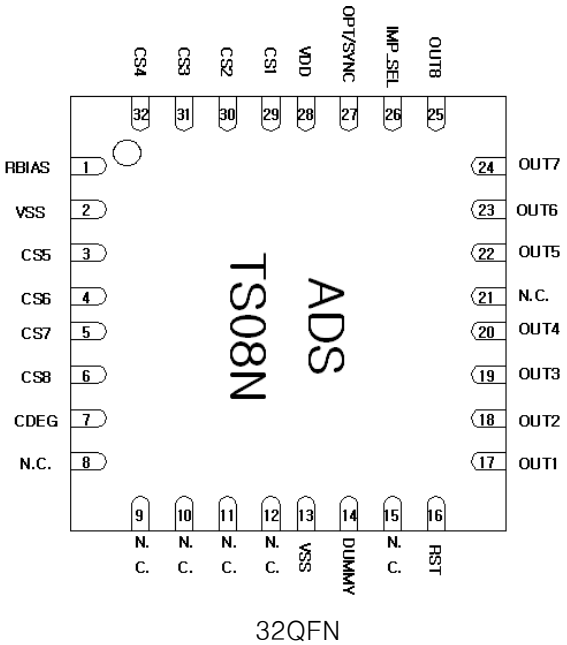
1.2 Application

- Home application
- Membrane switch replacement
- Sealed control panels, keypads
- Door key-lock matrix application
- Touch screen replacement application

1.3 Package (24SOP / 32QFN)



24SOP



32QFN

※ Drawings not to scale

2 Pin Description

2.1 24SOP package

PIN Number	Name	I/O	Description	Protection
1	CS6	Analog Input	CH6 capacitive sensor input	VDD/GND
2	CS7	Analog Input	CH7 capacitive sensor input	VDD/GND
3	CS8	Analog Input	CH8 capacitive sensor input	VDD/GND
4	CDEG	Analog Input	3 step sensitivity level selection	VDD/GND
5	N.C.	–	–	–
6	VSS	Ground	Supply ground	VDD
7	RST	Digital Input	System reset (High reset)	VDD/GND
8	OUT1	Digital Output	CH1 output (Open drain)	VDD/GND
9	OUT2	Digital Output	CH2 output (Open drain)	VDD/GND
10	OUT3	Digital Output	CH3 output (Open drain)	VDD/GND
11	OUT4	Digital Output	CH4 output (Open drain)	VDD/GND
12	OUT5	Digital Output	CH5 output (Open drain)	VDD/GND
13	OUT6	Digital Output	CH6 output (Open drain)	VDD/GND
14	OUT7	Digital Output	CH7 output (Open drain)	VDD/GND
15	OUT8	Digital Output	CH8 output (Open drain)	VDD/GND
16	IMP_SEL	Digital Input	Sense line impedance selection (Note 1)	VDD/GND
17	SYNC/OPT	Analog Input/Output	Output mode selection (Single Output / Multi Output) (Note 2) Sync pulse input /output	VDD/GND
18	VDD	Power	Power (2.5V~5.0V)	GND
19	CS1	Analog Input	CH1 capacitive sensor input	VDD/GND
20	CS2	Analog Input	CH2 capacitive sensor input	VDD/GND
21	CS3	Analog Input	CH3 capacitive sensor input	VDD/GND
22	CS4	Analog Input	CH4 capacitive sensor input	VDD/GND
23	R_BIAS	Analog Input	Internal bias adjust input	VDD/GND
24	CS5	Analog Input	CH5 capacitive sensor input	VDD/GND

Note 1 : Refer to 6.7 IMP_SEL (Sense Line Impedance) Implementation
Note 2 : Refer to 6.4 SYNC/OPT implementation

2.2 32QFN package

PIN No.	Name	I/O	Description	Protection
1	RBIAS	Analog Input	Internal bias adjust input	VDD/GND
2	VSS	Analog Input	–	VDD/GND
3	CS5	Analog Input	CH5 capacitive sensor input	VDD/GND
4	CS6	Analog Input	CH6 capacitive sensor input	VDD/GND
5	CS7	Analog Input	CH7 capacitive sensor input	VDD/GND
6	CS8	Analog Input	CH8 capacitive sensor input	VDD/GND
7	CDEG	Analog Input	3 step sensitivity level selection	VDD/GND
8	N.C.	–	No Connection	–
9	N.C.	–	No Connection	–
10	N.C.	–	No Connection	–
11	N.C.	–	No Connection	–
12	N.C.	–	No Connection	–
13	VSS	Ground	Supply ground	VDD
14	DUMMY	–	No Connection (Note 3)	–
15	N.C.	–	No Connection	–
16	RST	Digital Input	System reset (High reset)	VDD/GND
17	OUT1	Digital Output	CH1 output (Open drain)	VDD/GND
18	OUT2	Digital Output	CH2 output (Open drain)	VDD/GND
19	OUT3	Digital Output	CH3 output (Open drain)	VDD/GND
20	OUT4	Digital Output	CH4 output (Open drain)	VDD/GND
21	N.C.	–	No Connection	–
22	OUT5	Digital Output	CH5 output (Open drain)	VDD/GND
23	OUT6	Digital Output	CH6 output (Open drain)	VDD/GND
24	OUT7	Digital Output	CH7 output (Open drain)	VDD/GND
25	OUT8	Digital Output	CH8 output (Open drain)	VDD/GND
26	IMP_SEL	Digital Input	Sense line impedance selection (Note 1)	VDD/GND
27	SYNC/OPT	Digital Input/Output	Output mode selection (Single Output / Multi Output) (Note 2) Sync pulse input /output	VDD/GND
28	VDD	Power	Power (2.5V~5.0V)	GND
29	CS1	Analog Input	CH1 capacitive sensor input	VDD/GND
30	CS2	Analog Input	CH2 capacitive sensor input	VDD/GND
31	CS3	Analog Input	CH3 capacitive sensor input	VDD/GND
32	CS4	Analog Input	CH4 capacitive sensor input	VDD/GND

Note 3 : DUMMY pin should be no connection.

3 Absolute Maximum Rating

Battery supply voltage	5.5V
Maximum voltage on any pin	VDD+0.3
Maximum current on any PAD	100mA
Power Dissipation	800mW
Storage Temperature	−50 ~ 150℃
Operating Temperature	−20 ~ 75℃
Junction Temperature	150℃

Note Unless any other command is noted, all above are operated in normal temperature.

4 ESD & Latch-up Characteristics

4.1 ESD Characteristics

Mode	Polarity	Max	Reference
H.B.M	Pos / Neg	8000V	VDD
		8000V	VSS
		8000V	P to P
M.M	Pos / Neg	400V	VDD
		400V	VSS
		400V	P to P
C.D.M	Pos / Neg	800V	DIRECT
		800V	

4.2 Latch-up Characteristics

Mode	Polarity	Max	Test Step
I Test	Positive	200mA	25mA
	Negative	−200mA	
V supply over 5.0V	Positive	8.25V	1.0V

5 Electrical Characteristics (Preliminary)

▪ V_{DD}=3.3V, Rb=510k, (Unless otherwise noted), T_A = 25℃

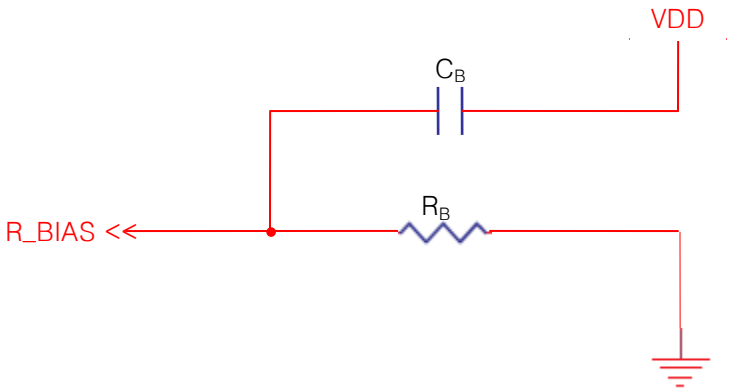
Characteristics	Symbol	Test Condition	Min	Typ	Max	Units
Operating supply voltage	V_{DD}		2.5	3.3	5.0	V
Current consumption	I_{DD}	V_{DD}= 3.3V R_B=510k	–	100		μA
		V_{DD}= 5.0V R_B=510k	–	170		
Output maximum sink current	I_{OUT}	T_A = 25℃	–	–	4.0	mA
Sense input capacitance range Note4	C_S		–	10	100	pF
Sense input resistance range	R_S		–	200	1000	Ω
Minimum detective capacitance difference	ΔC	Cs = 10pF, C_{DEG} Short to GND	0.2	–	–	pF
		Cs = 10pF, C_{DEG} Open	0.3	–	–	
Output impedance (open drain)	Zo	ΔC > 0.2pF, Cs = 10pF, C_{DEG} = 200pF	–	12	–	Ω
		ΔC < 0.2pF, Cs = 10pF, C_{DEG} = 200pF	–	30M	–	
Self calibration time after system reset	T_{CAL}	V_{DD} = 3.3V R_B = 510k	–	100	–	ms
		V_{DD} = 5.0V R_B = 510k	–	80	–	
Recommended bias resistance range Note5	R_B	V_{DD} = 2.5V	100	200	470	kΩ
		V_{DD} = 3.3V	200	330	680	
		V_{DD} = 5.0V	300	510	1000	
Maximum bias capacitance	C_{B_MAX}		–	820	1000	pF
Recommended sync resistance range	R_{SYNC}		1	2	20	MΩ
Sensitivity level selection	C_{DEG}	High sensitivity	Short			pF
		Normal sensitivity	Open			

Note 4: The sensitivity can be increased with lower C_S value.
The recommended value of C_S is 10pF when using 3T PC(Poly Carbonate) cover and 10 ㎜ x 7 ㎜ touch pattern.

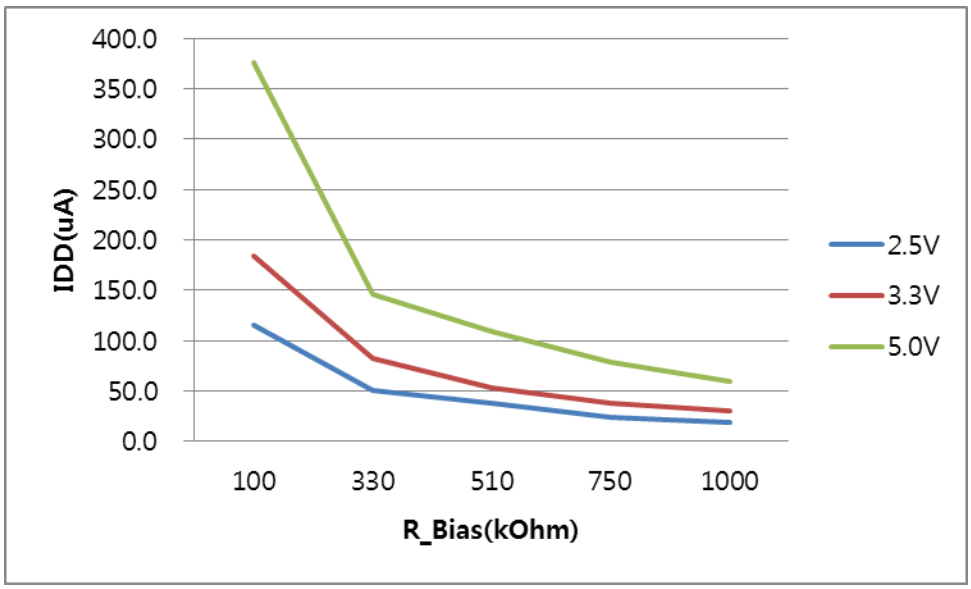
Note 5: The lower R_B is recommended in noisy condition.

6 TS08N Implementation

6.1 R_BIAS implementation



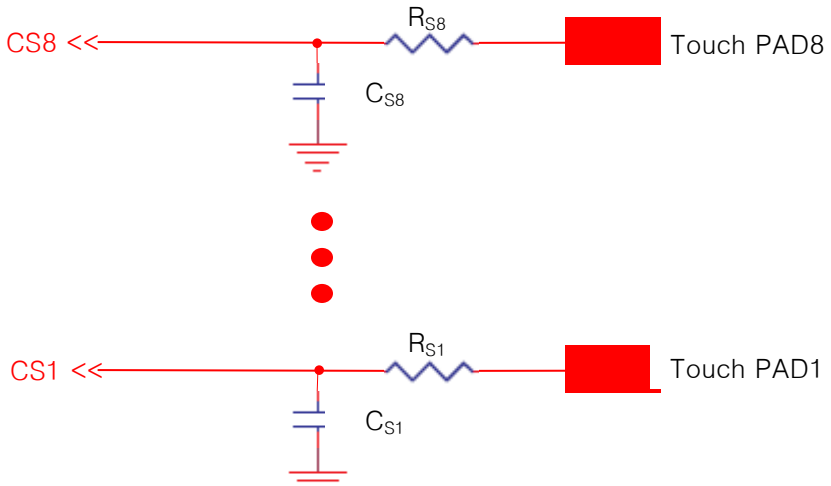
The R_BIAS is connected to the resistor to decide the oscillator and internal bias current. The sensing frequency, internal clock frequency and current consumption are therefore able to be adjusted with R_B. A voltage ripple on R_BIAS can make critical internal error, so C_B is connected to the VDD (not GND) is recommended. (The typical value of C_B is 820pF and the maximum Value is 1nF.)



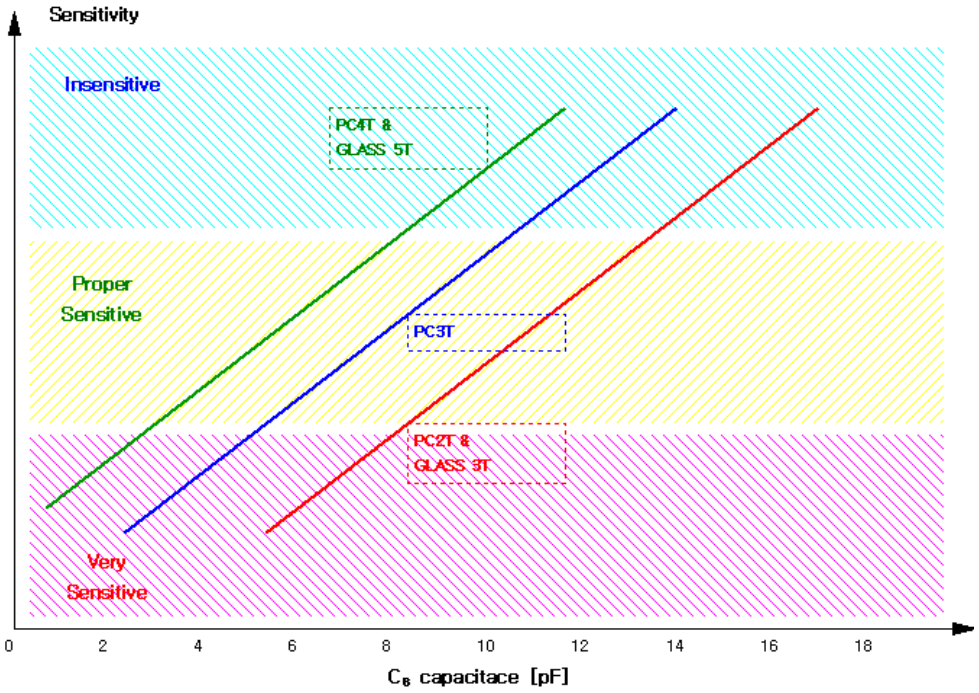
Normal operation current consumption curve

The current consumption curve of TS08N is represented in accordance with R_B value as above. The lower R_B requires more current consumption but it is recommended in noisy application. For example, refrigerator, air conditioner and so on.

6.2 CS implementation

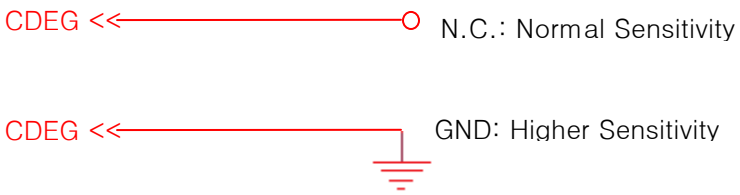


The parallel capacitor C_{S1} is added t 1 and C_{S8} to CS8 to adjust sensitivity. The sensitivity will be increased when smaller value of C_S is used. (Refer to the below Sensitivity Example Figure) It could be useful in case detail sensitivity mediation is required. The TS08N has three steps sensitivity and it is available to control with CDEG pin. (Refer to 6.3 CDEG implementation chapters) The TS08N has eight independent touch sensor input from CS1 to CS8. The internal touch decision process of each channel is separated from each other. Therefore eight channel touch key board application can be designed by using only one TS08N without coupling problem. The R_S is serial connection resistor to avoid mal-function from external surge and ESD. (It might be optional.) From 200Ω to 1kΩ is recommended for R_S. The size and shape of PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10 ㎜ x 7 ㎜). The connection line of CS1 and CS2 to touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detect caused by connection line.



Sensitivity example figure at High sensitivity

6.3 CDEG implementation



The TS08N has internal threshold levels to detect the capacitance variation for the decision of touching. The one of two step sensitivity is decided by CDEG pin connection. The sensitivity is decided by CDEG pin as below table. The high sensitivity is not recommended in noisy applications.

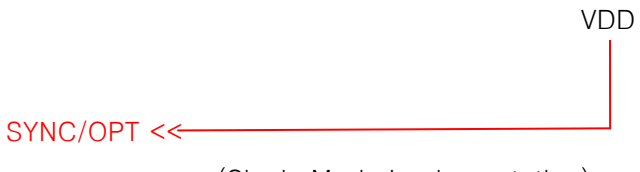
CDEG Connection vs. sensitivity

Sensitivity Level	Normal	High
CDEG Connection	Not Connect	Connect to GND

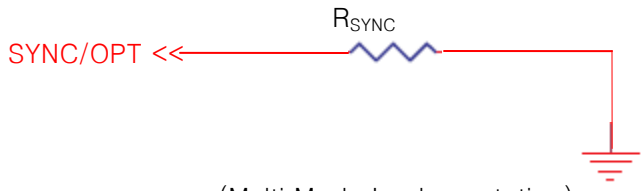
6.4 SYNC/OPT implementation

6.4.1 Single Connection

This pin will be assigned for the output option selection. It will decide that TS08N is working on single or multi touch detection mode. It should be implemented as below for these.



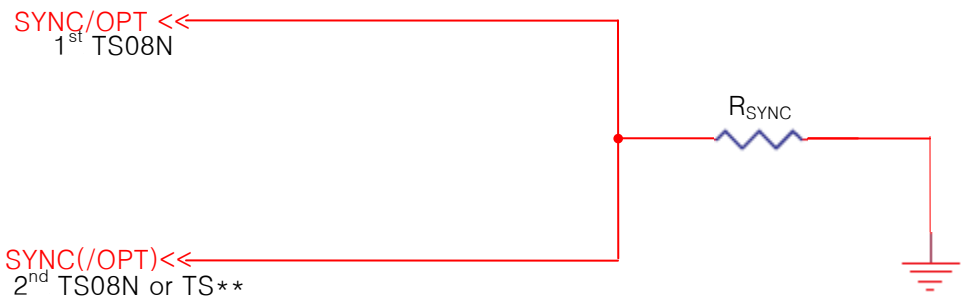
(Single Mode Implementation)



(Multi Mode Implementation)

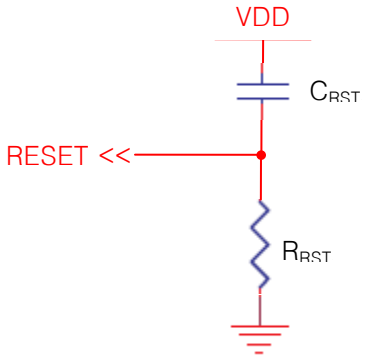
6.4.2 Multi Connection

Over two TS08N can work on the one application at the same time thanks to SYNC function with this pin. The SYNC pulse prevents over two sensing signal from interfering with each other. R_{SYNC} is pull-down resistor of SYNC/OPT pin. Too big value of R_{SYNC} makes the SYNC pulse falling delay, and too small value of R_{SYNC} makes rising delay. Typical value of R_{SYNC} is 2MΩ.The Sync pin should be implemented as below. The TS08N can also be used with the other TSxx series by employing this SYNC function. The TS08N could only operate on multi output mode in this configuration.



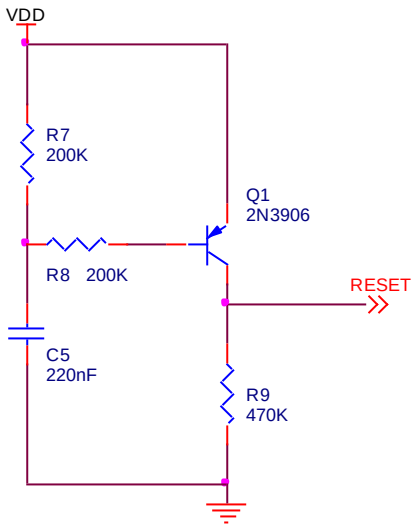
6.5 RESET implementation

TS08N has internal data latches, so initial state of these latches must be reset by external reset pulse before normal operation starts. The reset pulse can be controlled by host MCU directly or other reset device. If not, the circuit should be composed as below figure. The reset pulse must have high pulse duration about a few msec to cover power VDD rising time. The recommended value of R_{RST} and C_{RST} are 330KΩ and 100nF.



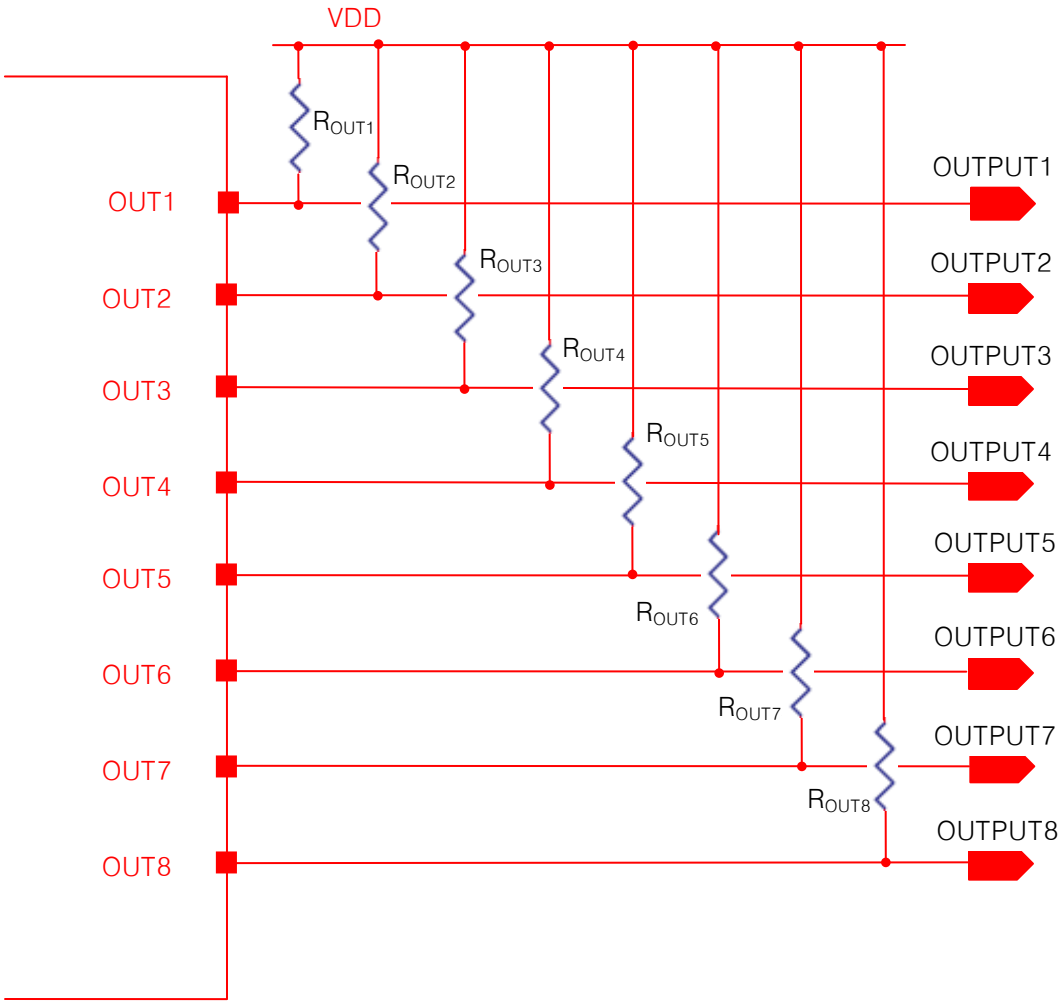
Recommended reset circuits 1

The better performance is warranted with below reset circuit. The Q1 is turned on and makes reset pulse when power is on and VDD is raised to operating voltage. After a few msec (duration time is determined by R7, R8, C5), Q1 is turned off and TS08N can be operated with normal sensitivity.



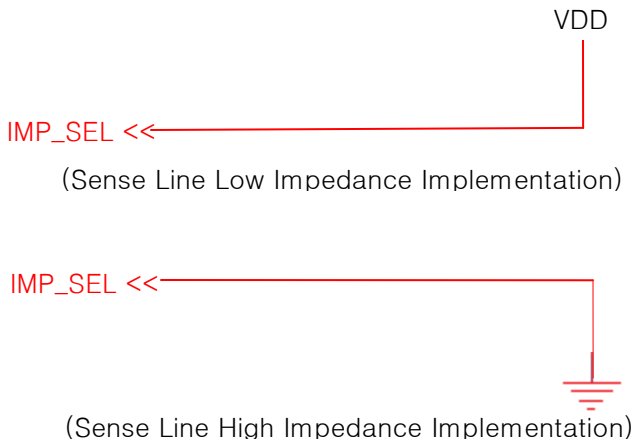
Recommended reset circuits 2

6.6 Output Circuit Implementation



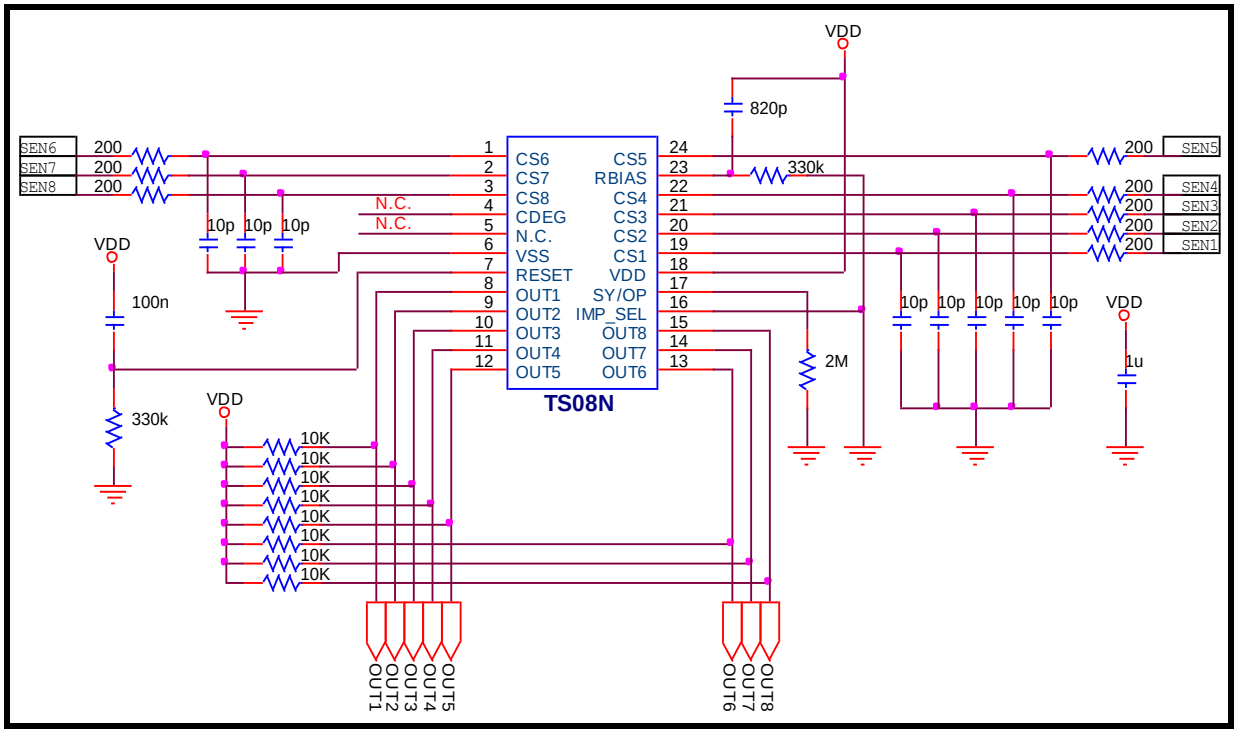
The OUTPUT pins have an open drain structure. For this reason, the connection of pull-up resistor R_{OUT} is required between OUTPUT and VDD. The maximum output sink current is 4mA, so over a few kΩ must be used as R_{OUT}. Normally 10kΩ is used as R_{OUT}.
The OUTPUT is high in normal situation, and the value is low when a touch is detected on the corresponding CS.

6.7 IMP_SEL (Sense Line Impedance) Implementation



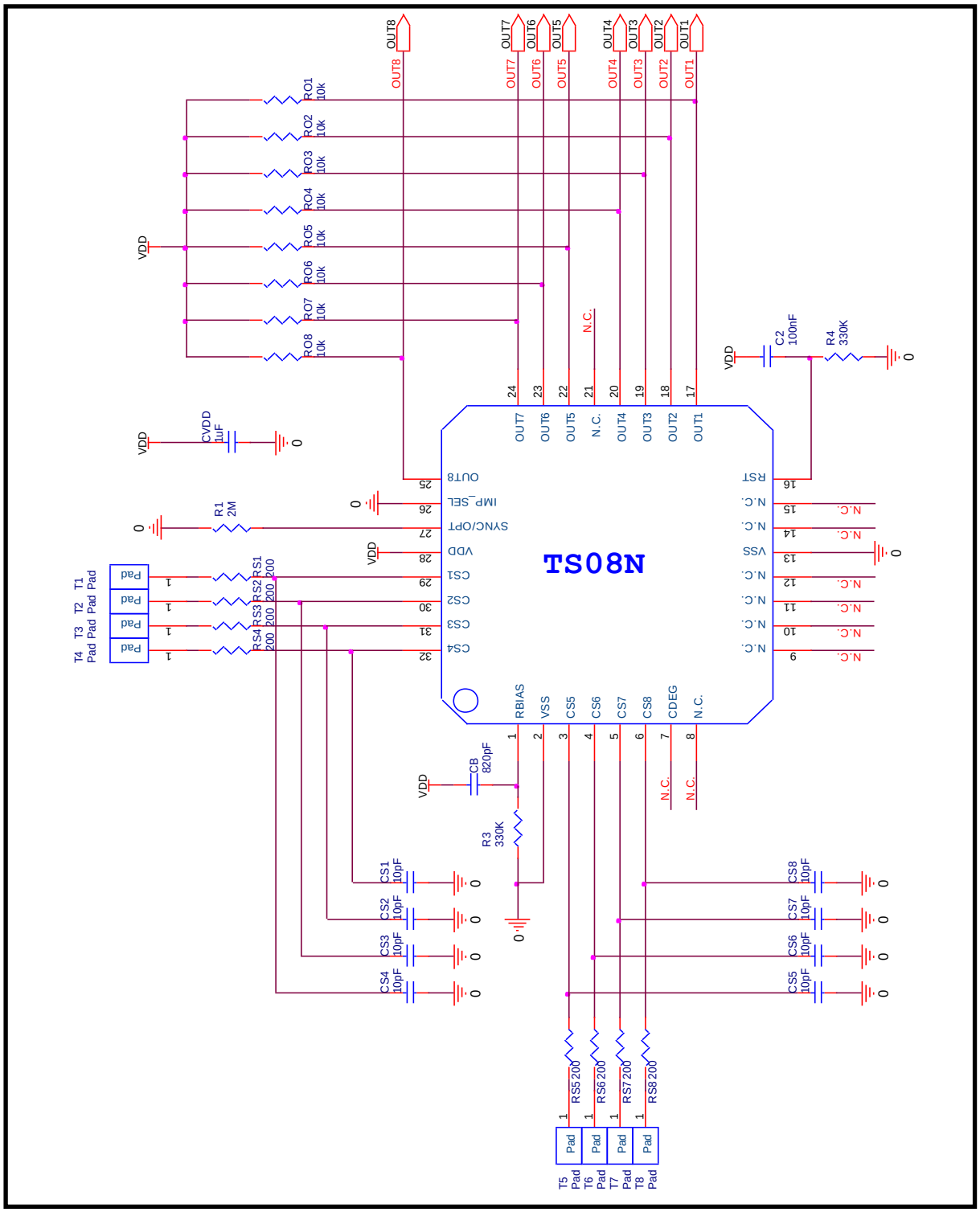
The sense input impedance might be selected by the IMP_SEL pin. In case of multi channel touch sensor application, the sense lines could be drawing side by side with very small gap. In this case, the sensitivity could be affected by the neighbor channel during out of scanning. Therefore the connection of IM_SEL pin is recommended to connect with VDD (low impedance mode). In the other case, the high impedance mode (connection with GND) has an advantage for sensitivity.

7 Recommended Circuit Diagram



TS08N(24SOP) Application Example Circuit

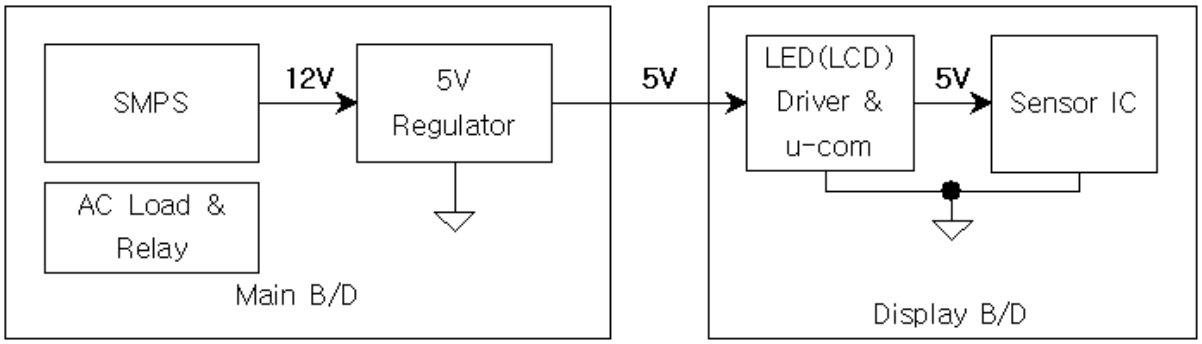
- The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of TS08N should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from that of TS08N.
- When TS08N used in noisy environment, lower R_B resistor is recommended.
- In PCB layout, RBIAS pattern should not be placed on touch pattern. If not, C_B has to be connected. The RBIAS pattern should be routed as short as possible.
- The CS patterns also should be routed as short as possible and the width of the line might be about 0.25mm.
- The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from TS08N.
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.
- The sensitivity can be changed by connection of CDEG. (See 6.3 CDEG implementation chapter)
- The TS08N is reset if RESET pin is high. (See 6.5 Reset implementation chapter)
- The OUT1 ~ OUT8 are open drain output ports. Therefore the pull-up resistor should be needed as above figure.
- The TS08N is working with single output mode if SYNC pin is high and it will be in multi output mode when SYNC pin is low. The resistor (2MΩ) which is connected SYNC pin to GND is required for SYNC operation.(See 6.4 SYNC/OPT implementation)
- Unused CS pins may be connected to GND for stable operation. In that case TS08N operates in fast sensing mode and needs more current.



TS08N(32QFN) Application Example Circuit

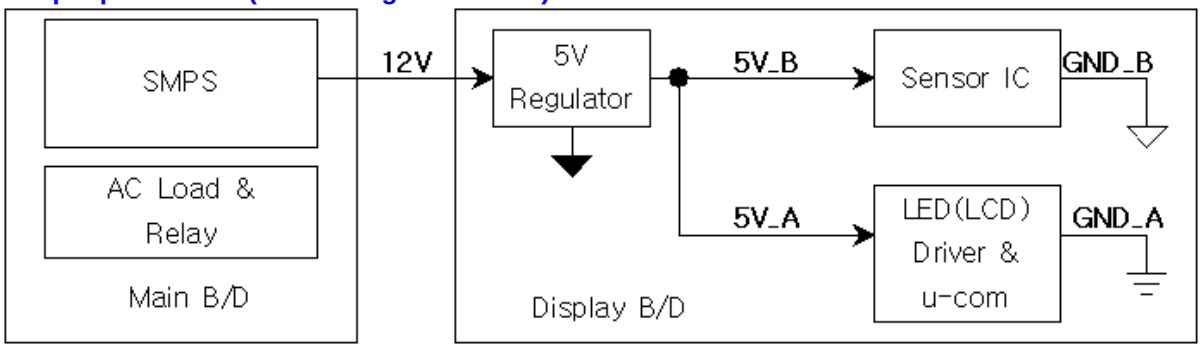
7.1 Example – Power Line Split Strategy PCB Layout

A. Not split power Line (Bad power line design)

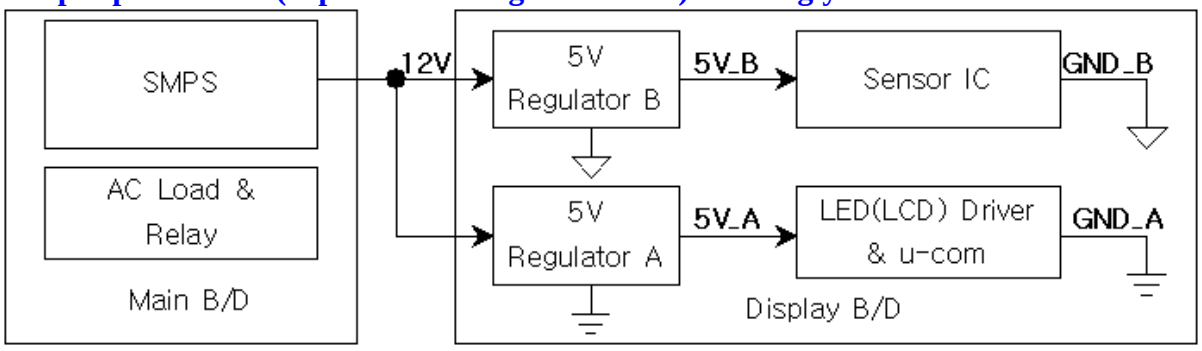


- The noise that is generated by AC load or relay can be loaded at 5V power line.
- A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD (5V).

B. Split power Line (One 5V regulator used) – Recommended

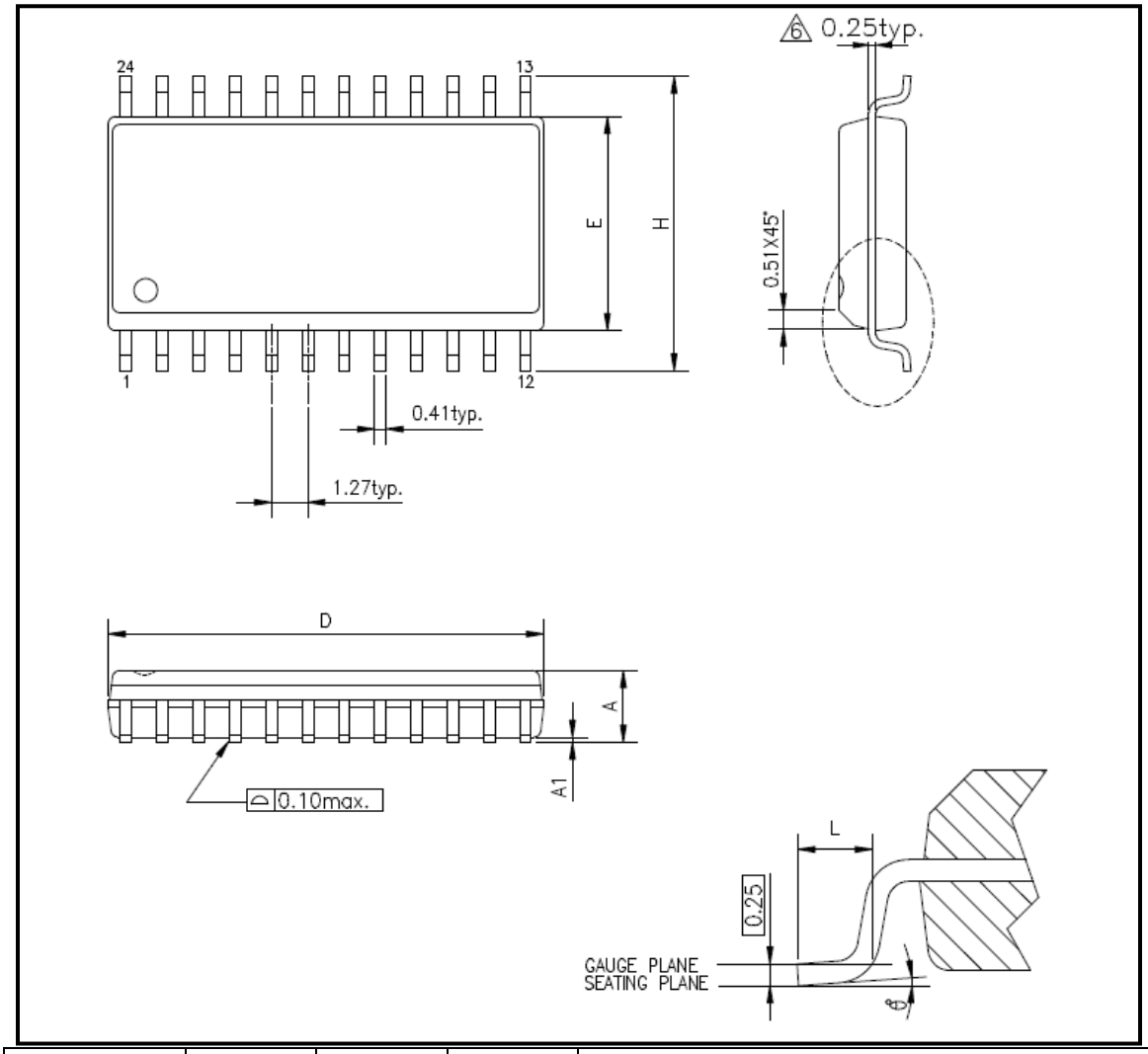


C. Split power Line (Separated 5V regulator used) – Strongly recommended



8 MECHANICAL DRAWING

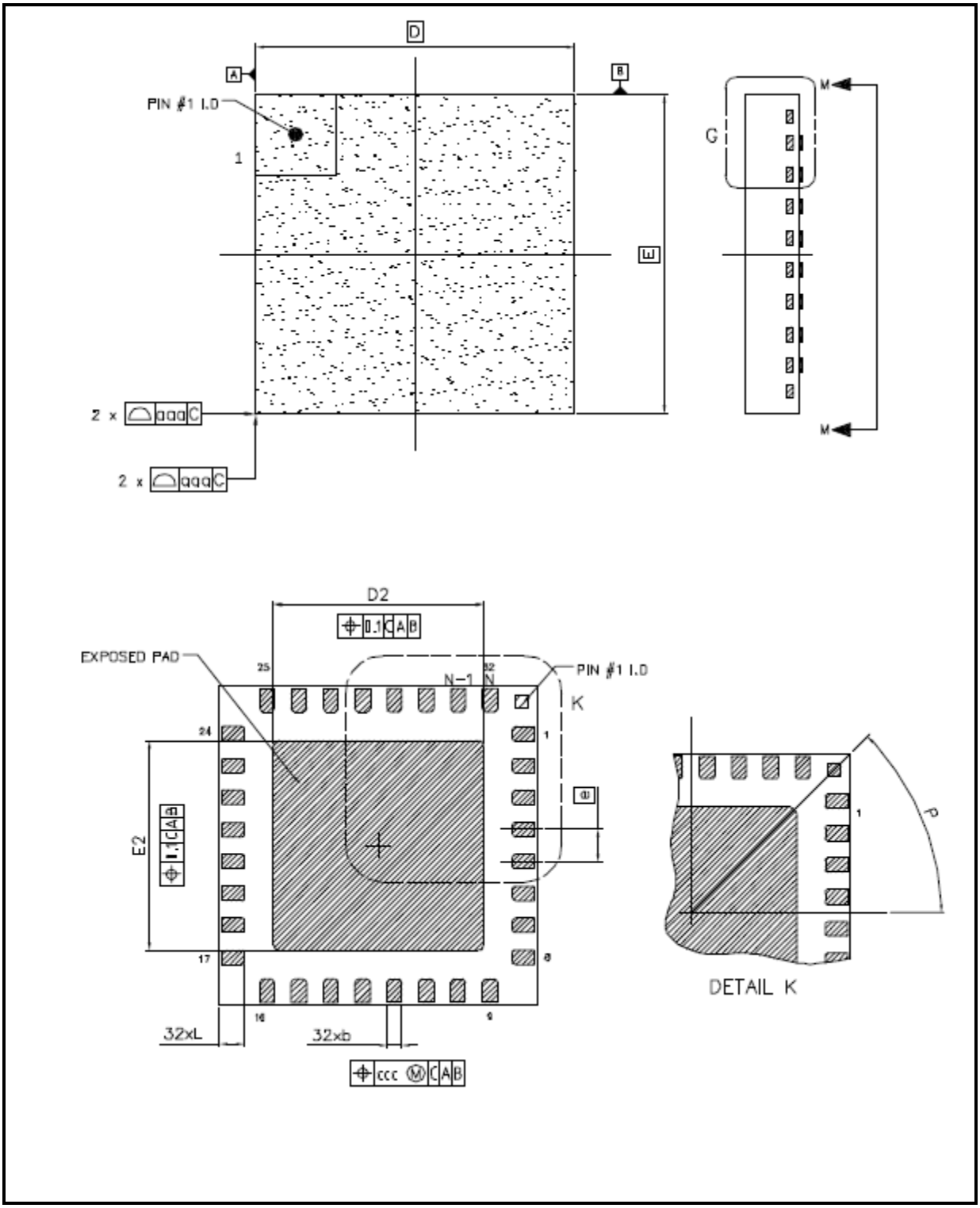
8.1 Mechanical Drawing (24 SOP)

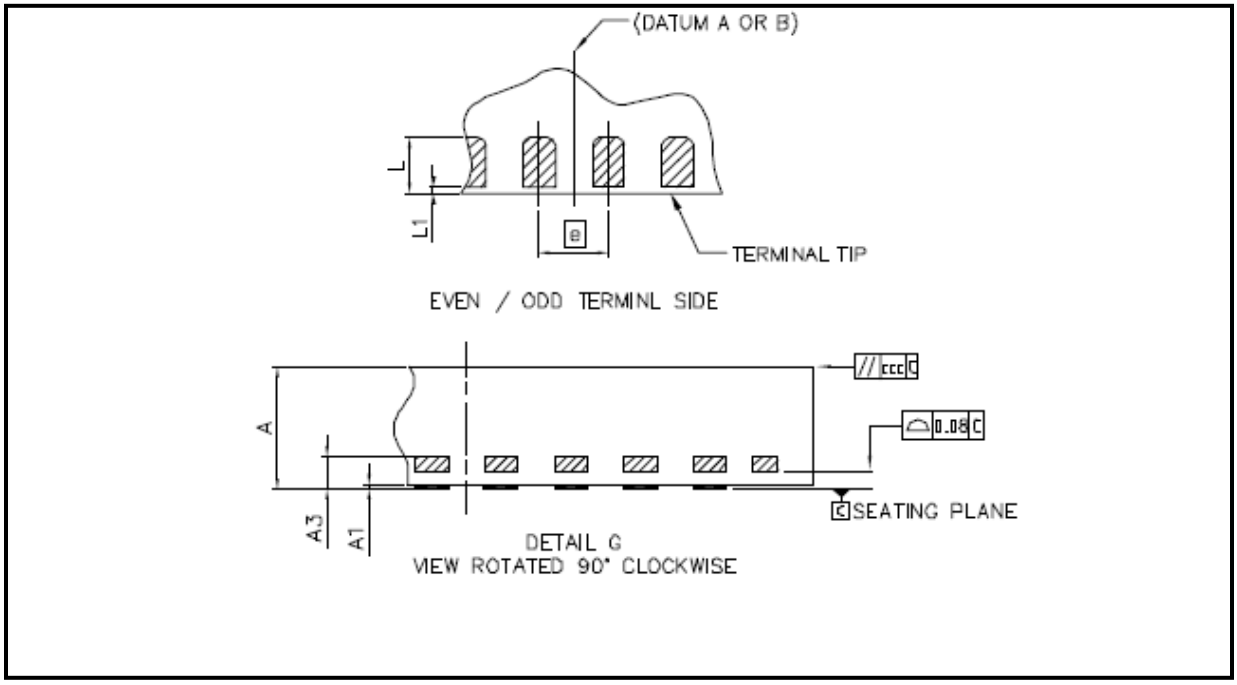


SYMBOLS	MIN.	NOM.	MAX.	NOTES
A	-	-	2.64	1. JEDEC OUTLINE : N/A. 2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .25mm (.010in) PER SIDE 3. DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.
A1	0.10	-	-	
D	15.24	-	15.70	
E	7.42	7.52	7.59	
H	10.29	10.46	10.64	
L	0.53	0.79	1.04	
θ°	0	4	8	

UNIT : mm

8.2 Mechanical Drawing (32 QFN)





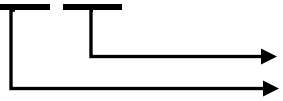
DIM	MIN	NOM	MAX	NOTES
A	0.80	0.85	0.90	1. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES. 2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE. 3. COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL. 4. RADIUS ON TERMINAL IS OPTIONAL.
A1	0.00		0.05	
A3	0.203 REF			
b	0.18	0.23	0.30	
D	5.00 BSC			
E	5.00 BSC			
D2	3.20	3.30	3.40	
E2	3.20	3.30	3.40	
e	0.50 BSC			
L	0.35	0.40	0.45	
L1	-	-	0.10	
P		45° BSC		
aaa		0.15		
ccc		0.10		

9 MARKING DESCRIPTION

Device Code : **T S 0 8 NC**

Type of version
Channel Number
Touch Switch Group

Weekly Code : **YY ZZ**



Manufacturing Week
Manufacturing Year

NOTES:

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