ad semiconductor

TS20

20-Ch Auto Sensitivity Calibration Capacitive Touch Sensor

SPECIFICATION V1.3

March 2009

ADSemiconductor

1 Specification

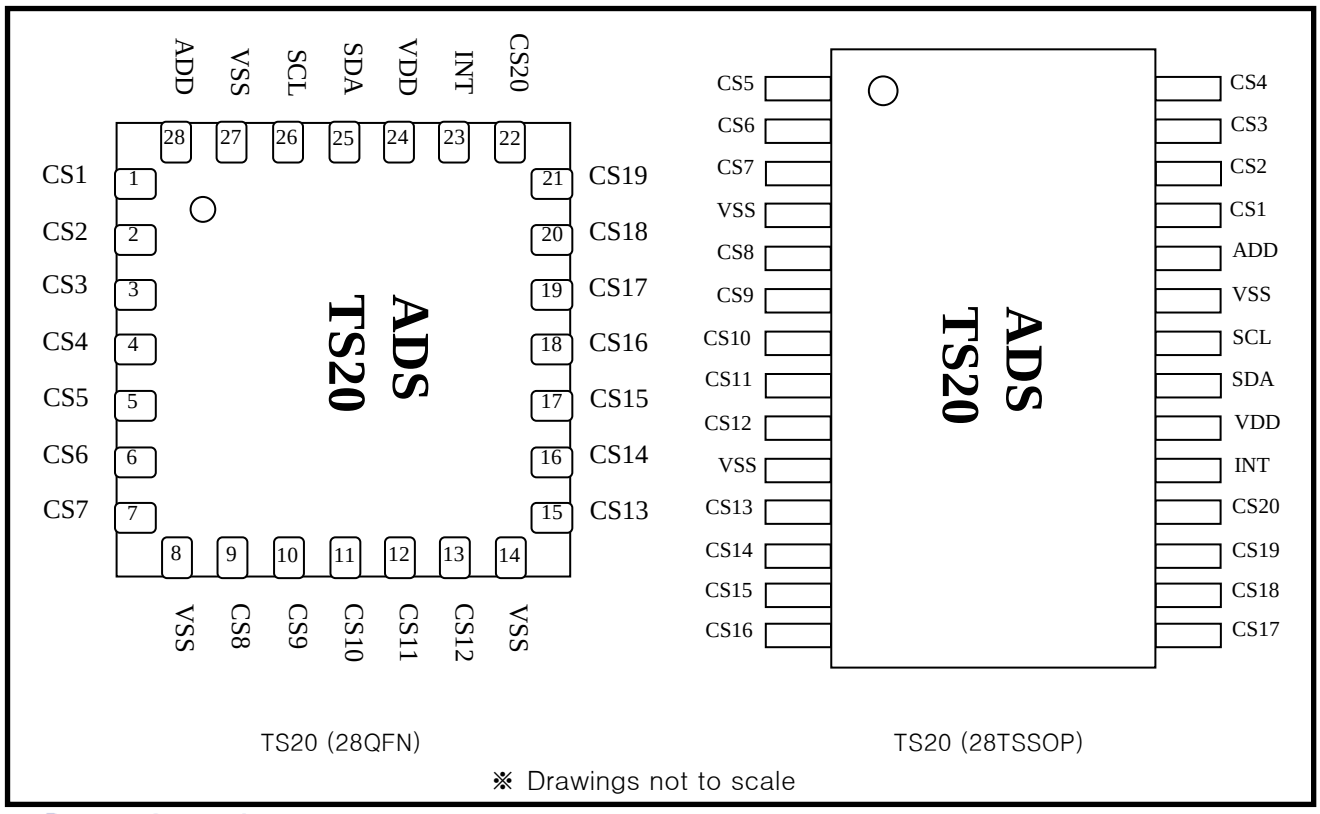
1.1 General Feature

- 20-Channel capacitive sensor with auto sensitivity calibration
- I^2C serial interface
- Selectable output operation (single mode / multi-mode)
- Independently adjustable in 16 steps (2 mode) sensitivity
- Adjustable response time by the control registers
- Embedded common and normal noise elimination circuit
- Available LED PWM drive ports up to 20 channels
- Controllable LED luminance
- Available tact switch input up to 20 channels
- SLEEP mode to save the current consumption
- RoHS compliant 28QFN and 28TSSOP package

1.2 Application

- Mobile application (mobile phone, PDA, PMP, MP3, Car navigation)
- Membrane switch replacement
- Sealed control panels, keypads
- Door key-lock matrix application
- Touch screen replacement application

1.3 Package (28 QFN / 28TSSOP)



TS20 (28QFN) TS20 (28TSSOP)

※ Drawings not to scale

2 Pin Description

2.1 TS20 (28QFN package)

PIN No.	Name	I/O	Description	Protection
1	CS1	Analog Input /Digital Output	CH1 capacitive sensor input CH1 Tact switch input [Note 2] CH1 LED Drive output (Open drain) [Note 3]	VDD/GND
2	CS2	Analog Input /Digital Output	CH2 capacitive sensor input CH2 Tact switch input [Note 2] CH2 LED Drive output (Open drain) [Note 3]	VDD/GND
3	CS3	Analog Input /Digital Output	CH3 capacitive sensor input CH3 Tact switch input [Note 2] CH3 LED Drive output (Open drain) [Note 3]	VDD/GND
4	CS4	Analog Input /Digital Output	CH4 capacitive sensor input CH4 Tact switch input [Note 2] CH4 LED Drive output (Open drain) [Note 3]	VDD/GND
5	CS5	Analog Input /Digital Output	CH5 capacitive sensor input CH5 Tact switch input [Note 2] CH5 LED Drive output (Open drain) [Note 3]	VDD/GND
6	CS6	Analog Input /Digital Output	CH6 capacitive sensor input CH6 Tact switch input [Note 2] CH6 LED Drive output (Open drain) [Note 3]	VDD/GND
7	CS7	Analog Input /Digital Output	CH7 capacitive sensor input CH7 Tact switch input [Note 2] CH7 LED Drive output (Open drain) [Note 3]	VDD/GND
8	VSS	Ground	Supply ground	VDD
9	CS8	Analog Input /Digital Output	CH8 capacitive sensor input CH8 Tact switch input [Note 2] CH8 LED Drive output (Open drain) [Note 3]	VDD/GND
10	CS9	Analog Input /Digital Output	CH9 capacitive sensor input CH9 Tact switch input [Note 2] CH9 LED Drive output (Open drain) [Note 3]	VDD/GND
11	CS10	Analog Input /Digital Output	CH10 capacitive sensor input CH10 Tact switch input [Note 2] CH10 LED Drive output (Open drain) [Note 3]	VDD/GND
12	CS11	Analog Input /Digital Output	CH11 capacitive sensor input CH11 Tact switch input [Note 2] CH11 LED Drive output (Open drain) [Note 3]	VDD/GND
13	CS12	Analog Input /Digital Output	CH12 capacitive sensor input CH12 Tact switch input [Note 2] CH12 LED Drive output (Open drain) [Note 3]	VDD/GND
14	VSS	Ground	Supply ground	VDD
15	CS13	Analog Input /Digital Output	CH13 capacitive sensor input CH13 Tact switch input [Note 2] CH13 LED Drive output (Open drain) [Note 3]	VDD/GND
16	CS14	Analog Input /Digital Output	CH14 capacitive sensor input CH14 Tact switch input [Note 2] CH14 LED Drive output (Open drain) [Note 3]	VDD/GND

17	CS15	Analog Input /Digital Output	CH15 capacitive sensor input CH15 Tact switch input [Note 2] CH15 LED Drive output (Open drain) [Note 3]	VDD/GND
18	CS16	Analog Input /Digital Output	CH16 capacitive sensor input CH16 Tact switch input [Note 2] CH16 LED Drive output (Open drain) [Note 3]	VDD/GND
19	CS17	Analog Input /Digital Output	CH17 capacitive sensor input CH17 Tact switch input [Note 2] CH17 LED Drive output (Open drain) [Note 3]	VDD/GND
20	CS18	Analog Input /Digital Output	CH18 capacitive sensor input CH18 Tact switch input [Note 2] CH18 LED Drive output (Open drain) [Note 3]	VDD/GND
21	CS19	Analog Input /Digital Output	CH19 capacitive sensor input CH19 Tact switch input [Note 2] CH19 LED Drive output (Open drain) [Note 3]	VDD/GND
22	CS20	Analog Input /Digital Output	CH20 capacitive sensor input CH20 Tact switch input [Note 2] CH20 LED Drive output (Open drain) [Note 3]	VDD/GND
23	INT	Digital Output	Interrupt output (Open drain)	VDD/GND
24	VDD	Power	Power (2.5V~5.0V)	GND
25	SDA	Digital Input/Output	I^2C data (Open drain)	VDD/GND
26	SCL	Digital Input	I^2C clock input	VDD/GND
27	VSS	Ground	Supply ground	VDD
28	ADD	Digital Input	I^2C slave ID selection input [Note 1]	VDD/GND

Note 1: Refer to chapter 7. I2C Interface.
Note 2: Refer to chapter 6.2 CS implementation for Tact switch input.
Note 3: Refer to chapter 6.3 CS implementation for LED drive output.

2.2 TS20 (28TSSOP package)

PIN No.	Name	I/O	Description	Protection
1	CS5	Analog Input /Digital Output	CH5 capacitive sensor input CH5 Tact switch input [Note 2] CH5 LED Drive output (Open drain) [Note 3]	VDD/GND
2	CS6	Analog Input /Digital Output	CH6 capacitive sensor input CH6 Tact switch input [Note 2] CH6 LED Drive output (Open drain) [Note 3]	VDD/GND
3	CS7	Analog Input /Digital Output	CH7 capacitive sensor input CH7 Tact switch input [Note 2] CH7 LED Drive output (Open drain) [Note 3]	VDD/GND
4	VSS	Ground	Supply ground	VDD
5	CS8	Analog Input /Digital Output	CH8 capacitive sensor input CH8 Tact switch input [Note 2] CH8 LED Drive output (Open drain) [Note 3]	VDD/GND
6	CS9	Analog Input /Digital Output	CH9 capacitive sensor input CH9 Tact switch input [Note 2] CH9 LED Drive output (Open drain) [Note 3]	VDD/GND
7	CS10	Analog Input /Digital Output	CH10 capacitive sensor input CH10 Tact switch input [Note 2] CH10 LED Drive output (Open drain) [Note 3]	VDD/GND
8	CS11	Analog Input /Digital Output	CH11 capacitive sensor input CH11 Tact switch input [Note 2] CH11 LED Drive output (Open drain) [Note 3]	VDD/GND
9	CS12	Analog Input /Digital Output	CH12 capacitive sensor input CH12 Tact switch input [Note 2] CH12 LED Drive output (Open drain) [Note 3]	VDD/GND
10	VSS	Ground	Supply ground	VDD
11	CS13	Analog Input /Digital Output	CH13 capacitive sensor input CH13 Tact switch input [Note 2] CH13 LED Drive output (Open drain) [Note 3]	VDD/GND
12	CS14	Analog Input /Digital Output	CH14 capacitive sensor input CH14 Tact switch input [Note 2] CH14 LED Drive output (Open drain) [Note 3]	VDD/GND
13	CS15	Analog Input /Digital Output	CH15 capacitive sensor input CH15 Tact switch input [Note 2] CH15 LED Drive output (Open drain) [Note 3]	VDD/GND
14	CS16	Analog Input /Digital Output	CH16 capacitive sensor input CH16 Tact switch input [Note 2] CH16 LED Drive output (Open drain) [Note 3]	VDD/GND
15	CS17	Analog Input /Digital Output	CH17 capacitive sensor input CH17 Tact switch input [Note 2] CH17 LED Drive output (Open drain) [Note 3]	VDD/GND
16	CS18	Analog Input /Digital Output	CH18 capacitive sensor input CH18 Tact switch input [Note 2]	VDD/GND

			CH18 LED Drive output (Open drain) [Note 3]	
17	CS19	Analog Input /Digital Output	CH19 capacitive sensor input CH19 Tact switch input [Note 2] CH19 LED Drive output (Open drain) [Note 3]	VDD/GND
18	CS20	Analog Input /Digital Output	CH20 capacitive sensor input CH20 Tact switch input [Note 2] CH20 LED Drive output (Open drain) [Note 3]	VDD/GND
19	INT	Digital Output	Interrupt output (Open drain)	VDD/GND
20	VDD	Power	Power (2.5V~5.0V)	GND
21	SDA	Digital Input/Output	I^2C data (Open drain)	VDD/GND
22	SCL	Digital Input	I^2C clock input	VDD/GND
23	VSS	Ground	Supply ground	VDD
24	ADD	Digital Input	I^2C slave ID selection input [Note 1]	VDD/GND
25	CS1	Analog Input /Digital Output	CH1 capacitive sensor input CH1 Tact switch input [Note 2] CH1 LED Drive output (Open drain) [Note 3]	VDD/GND
26	CS2	Analog Input /Digital Output	CH2 capacitive sensor input CH2 Tact switch input [Note 2] CH2 LED Drive output (Open drain) [Note 3]	VDD/GND
27	CS3	Analog Input /Digital Output	CH3 capacitive sensor input CH3 Tact switch input [Note 2] CH3 LED Drive output (Open drain) [Note 3]	VDD/GND
28	CS4	Analog Input /Digital Output	CH4 capacitive sensor input CH4 Tact switch input [Note 2] CH4 LED Drive output (Open drain) [Note 3]	VDD/GND

Note 1: Refer to chapter 7. I2C Interface.
Note 2: Refer to chapter 6.2 CS implementation for Tact switch input.
Note 3: Refer to chapter 6.3 CS implementation for LED drive output.

3 Absolute Maximum Rating

Maximum supply voltage	5.5V
Maximum voltage on any pin	VDD+0.3
Maximum current on any PAD	100mA
Power Dissipation	800mW
Storage Temperature	−50 ~ 150℃
Operating Temperature	−20 ~ 75℃
Junction Temperature	150℃

Note Unless any other command is noted, all above are operated in normal temperature.

4 ESD & Latch-up Characteristics

4.1 ESD Characteristics

Mode	Polarity	Minimum Level	Reference
H.B.M	Pos / Neg	8000V	VDD
		8000V	GND
		8000V	P to P
M.M	Pos / Neg	625V	VDD
		625V	GND
		500V	P to P
C.D.M	-	1000V	Field Induced Charge

4.2 Latch-up Characteristics

Mode	Polarity	Minimum Level	Reference
I Test	Positive	100mA	JESD78A
	Negative	−100mA	
V supply over 5.0V	Positive	8.0V	

5 Electrical Characteristics

▪ V_{DD}=3.3V, T_A = 27℃

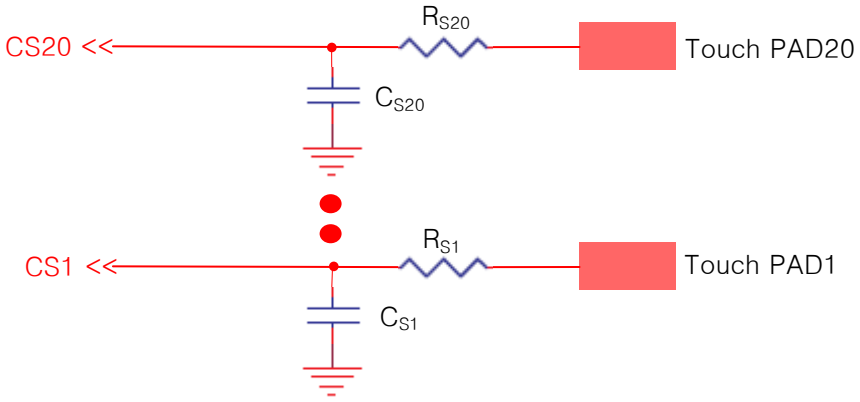
Characteristics	Symbol	Test Condition		Min	Typ	Max	Units
Operating supply voltage	V_{DD}			2.5	3.3	5.0	V
Current consumption [Note4]	I_{DD}	Slow mode	V_{DD}= 3.3V	–	85	–	μA
			V_{DD}= 5.0V	–	120	–	
		Normal mode	V_{DD}= 3.3V	–	130	180	
			V_{DD}= 5.0V		180	240	
		Fast mode	V_{DD}= 3.3V		190	–	
			V_{DD}= 5.0V	–	250	–	
		Sleep mode	V_{DD}= 3.3V	–	9	–	
			V_{DD}= 5.0V	–	11	–	
	I_{DD_I2C}	V_{DD}= 3.3V (2M Bps)		–	1.8	2.2	mA
		V_{DD}= 5.0V (2M Bps)		–	2.8	3.4	
Digital output maximum sink current	I_{OUT}	T_A = 25℃ (Normal I^2C Output)		–	–	4.0	mA
LED drive output sink current per 1channel	I_{LED_OUT}	T_A = 25℃ (LED Drive Output)		–	–	8.0	mA
LED drive output total sink current	I_{LED_TOT}	T_A = 25℃ (LED Drive Output)		–	–	30.0	mA
Tact switch interface input internal pull-up current	I_{TACT}	V_{DD}= 5.0V, T_A = 25℃		–	5.6	–	μA
Start supply voltage for internal reset	V_{DD_RST}	T_A = 25℃		–	–	0.3·V_{DD}	V
Sense input capacitance range [Note5]	C_S			–	–	50	pF
Minimum detective capacitance difference	ΔC_{MIN}			0.1	–	–	pF
Output impedance (open drain)	Zo	$\Delta C > \Delta C_{MIN}$		–	12	–	Ω
		$\Delta C < \Delta C_{MIN}$		–	30M	–	
Self calibration time after system reset	T_{CAL}	Slow calibration speed		–	100	–	ms
		Normal calibration speed		–	80	–	
		Fast calibration speed		–	60	–	
Sense input resistance	R_S	–		–	200	1000	Ω
Internal reset pulse duration	T_{RST}			2.5	–	–	usec
SCL, SDA rising delay	T_{SCL}, T_{SDA}			0	–	1	usec
Minimum power on SCL, SDA high time	T_{H_SCL}, T_{H_SDA}			100	–	–	msec

Note 4 : Maximum communication speed is 2Mbps.
Note 5 : The sensitivity can be decreased with higher parallel capacitance of CS pin including parasitic capacitance made by neighbor GND or other pattern. The series resistor(under 1kΩ) of CS can be used in noisy condition to avoid mal-function from external surge and ESD.

6 Implementation of TS20

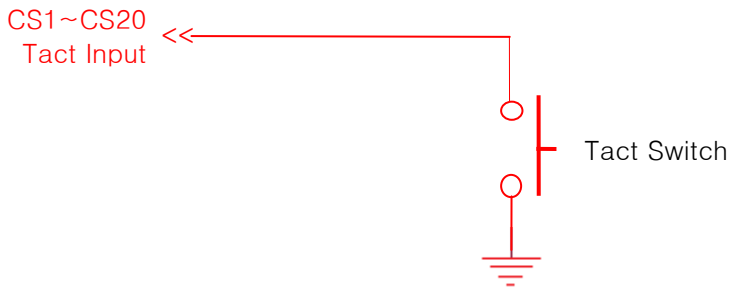
6.1 CS implementation

TS20 has 2 sensitivity modes and each mode has 16 step selections of the sensitivity. And Sensitivity of each sensing channel (CS) can be independently controlled by TS20 Control Register (I2C interface). External components of CS pin such as series resistor or parallel capacitor isn't necessary. The parallel parasitic capacitance of CS pins caused by touch line, touch pad and adjacent GND or other pattern may affect sensitivity. The sensitivity will be decreased when bigger parallel parasitic capacitance of CS pin is added.
Sensitivity mediation is required to complement sensitivity difference between channels. Parallel capacitor ($C_{S1\sim S20}$) of CS pin is useful in case of detail sensitivity mediation. The sensitivity would be increased when smaller value of C_S is used. Under 50pF capacitor can be used as sensitivity meditation capacitor and a few pF is usually used. The R_S, serial connection resistor of CS pins, may be used to avoid mal-function from external surge and ESD. (It might be optional.) From 200Ω to 1kΩ is recommended for R_S. Refer to below CS pins application figure.



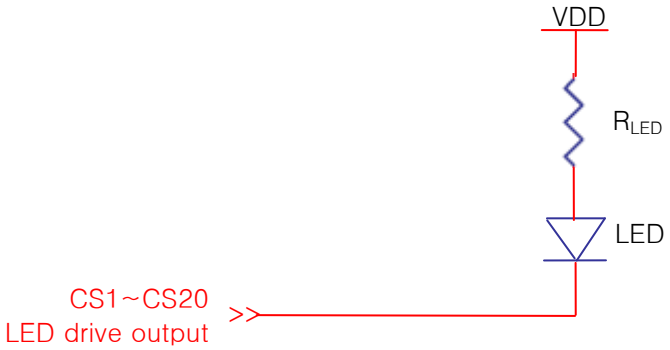
The TS20 has twenty independent touch sensor inputs from CS1 to CS20. The internal touch decision process of each channel is separated from others. Therefore twenty channel touch key board application can be designed by using only one TS20 without coupling problems.
The size and shape of PAD might have influence on the sensitivity. The sensitivity will be optimal when the size of PAD is approximately an half of the first knuckle (it's about 10㎜ x 7㎜). The connection line of CS to touch PAD is recommended to be routed as short as possible to prevent from abnormal touch detect caused by connection line.

6.2 CS implementation for tact switch input



CS input ports are possible to change to tact switch input by setting the Port Control Register[1] through I2C interface. The number of possible tact switch input is 20. And user can get the output data from output registers (Chapter 8.9). When the CS is used for tact switch input, the internal pull-up current source makes it possible without external pull-up resistors. Typical internal pull-up current is 5.6uA independent to external condition

6.3 CS implementation for LED drive output



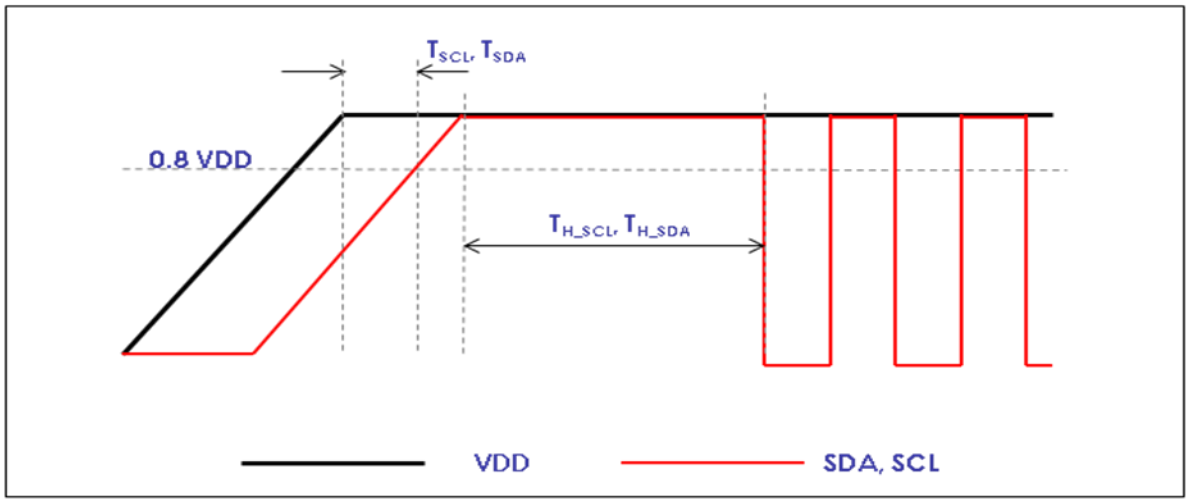
CS input ports are possible to change to LED drive output by setting the Port Control Register[2] through I2C interface. The number of possible LED drive output channel is 20. Each channel has 16 steps of LED dimming. Each LED dimming step is controlled by setting Port Control Register through I^2C interface. The maximum current that is sunk by CS is 8mA when the CS is used for LED drive output port.

[1] Refer to chapter 8.6 Port Control Register
[2] Refer to chapter 8.6 Port Control Register

6.4 Internal reset operation

The TS20 has stable internal reset circuit to offer reset pulse to digital block. The supply voltage for a system start or restart should be under $0.3 \cdot V_{DD}$ of normal operation V_{DD}. No external components required for TS20 power reset, that helps simple circuit design and to realize the low cost application.

6.5 Power on sequence for SCL & SDA



Timing Diagram

Items	Description	min	typ	max	unit
T_{SCL}	Settling time for SCL voltage rising to 0.8 VDD	0	-	1.0	usec
T_{SDA}	Settling time for SDA voltage rising to 0.8 VDD	0	-	1.0	usec
T_{H_SCL}, T_{H_SDA}	SCL SDA high pulse remain time for power on	100	-	-	msec

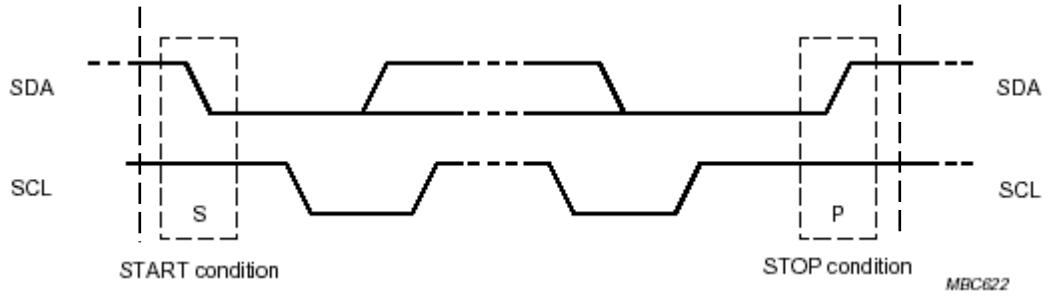
7 I2C Interface

7.1 I2C Enable / Disable

If the SDA or SCL signal goes to low, I2C control block is enabled automatically. And if the SDA and SCL signal maintain high during about 2 us, I2C control block is disabled automatically also.

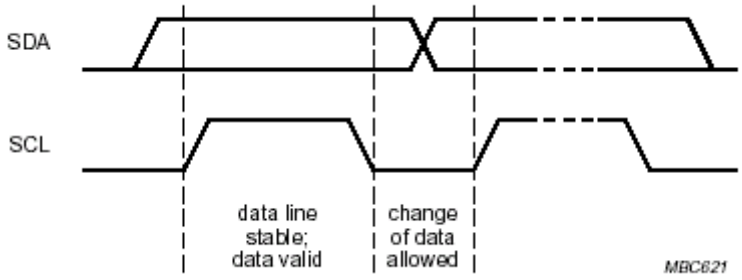
7.2 Start & Stop Condition

- Start Condition (S)
- Stop Condition (P)
- Repeated Start (Sr)



7.3 Data validity

The SDA should be stable when the SCL is high and the SDA can be changed when the SCL is low.

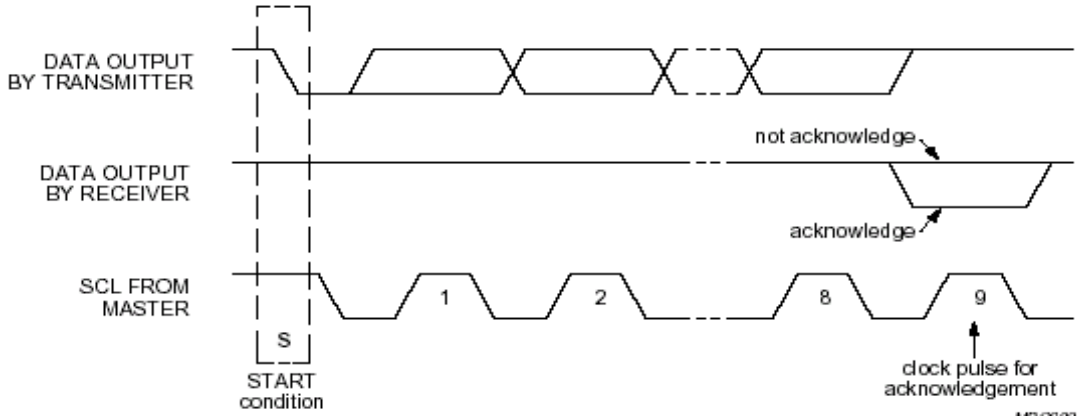


7.4 Byte Format

The byte structure is composed with 8Bit data and an acknowledge signal.

7.5 Acknowledge

It is a check bit whether the receiver gets the data from the transmitter without error or not. The receiver will write '0' when it received the data successfully and '1' if not.



7.6 First Byte

7.6.1 Slave Address

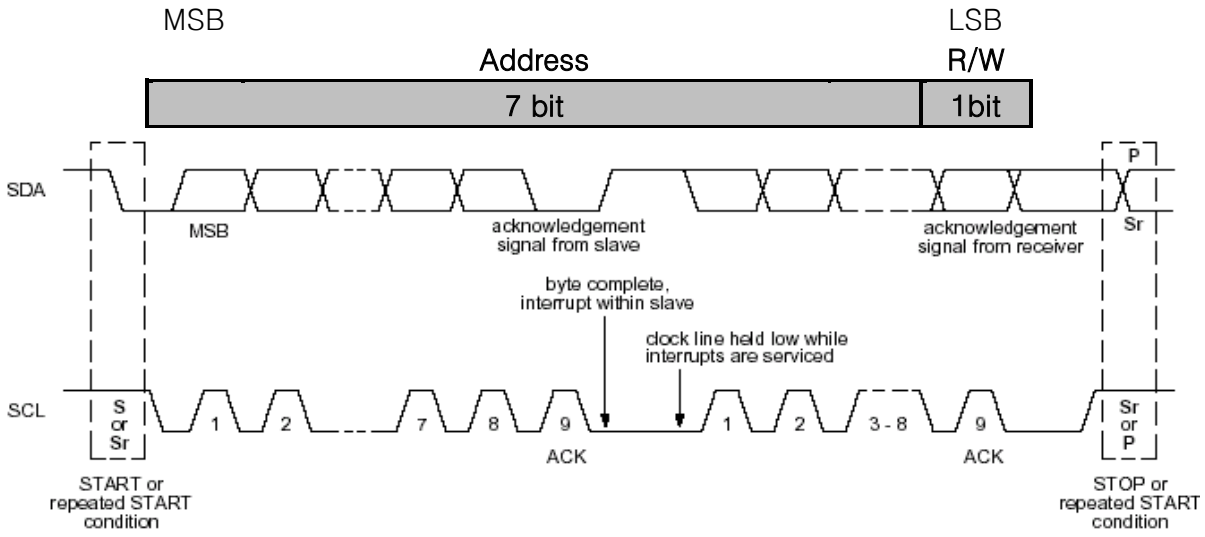
It is the first byte from the start condition. It is used to access the slave device.

TS20 Chip Address : 7bit

ADD	Address
GND	0xD4
VDD	0xF4

7.6.2 R/$\overline{W}$

The direction of data is decided by the bit and it follows the address data.

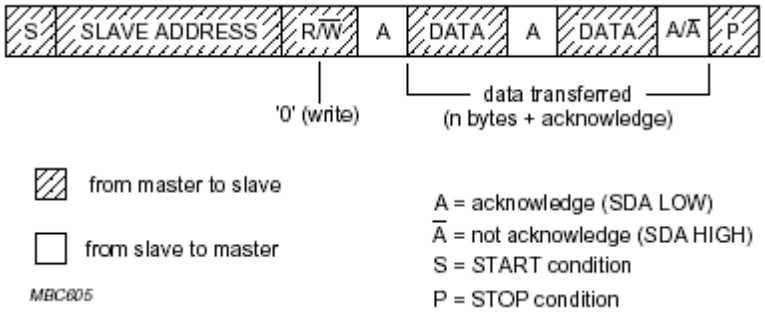


7.7 Transferring Data

7.7.1 Write Operation

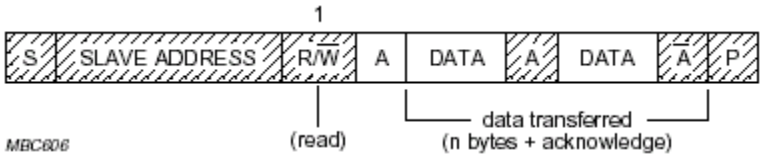
The byte sequence is as follows:

■ the first byte gives the device address plus the direction bit (R/W = 0).
■ the second byte contains the internal address of the first register to be accessed.
■ the next byte is written in the internal register. Following bytes are written in successive internal registers.
■ the transfer lasts until stop conditions are encountered.
■ the TS20 acknowledges every byte transfer.

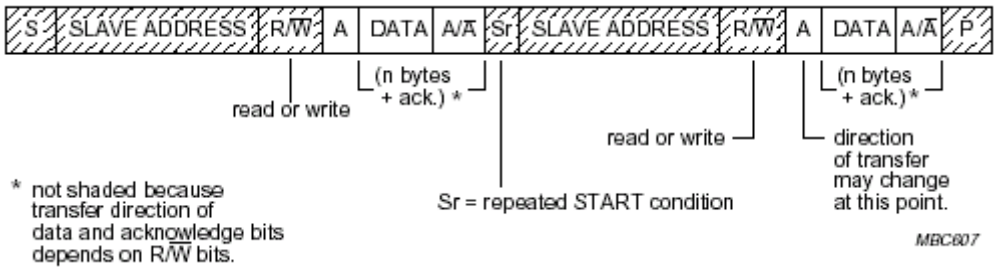


7.7.2 Read Operation

The address of the first register to read is programmed in a write operation without data, and terminated by the stop condition. Then, another start is followed by the device address and R/W= 1. All following bytes are now data to be read at successive positions starting from the initial address.



7.7.3 Read/Write Operation



7.8 I²C write and read operations in normal mode

The following figure represents the I²C normal mode write and read registers.

☞ Write register 0x00 to 0x01 with data AA and BB

Start	Device Address 0xD4	ACK	Register Address 0x00	ACK	Data AA	ACK	Data BB	ACK	Stop

Read register 0x00 and 0x01

Start	Device Address 0xD4	ACK	Register Address 0x00	ACK	Stop

Start	Device Address 0xD5	ACK	Data Read AA	ACK	Data Read BB	$\overline{\text{ACK}}$	Stop

From Master to Slave From Slave to Master

8 TS20 Control Register List

◀ Note: The unused bits (defined as reserved) in I²C registers must be kept to zero.

8.1 I²C Register Map

Name	Addr. (Hex)	Reset Value (Bin)	Register Function and Description							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Sensitivity/PWM1	00H	0101 0101	SEN_PWM_CH2				SEN_PWM_CH1			
Sensitivity/PWM2	01H	0101 0101	SEN_PWM_CH4				SEN_PWM_CH3			
Sensitivity/PWM3	02H	0101 0101	SEN_PWM_CH6				SEN_PWM_CH5			
Sensitivity/PWM4	03H	0101 0101	–				SEN_PWM_CH7			
Sensitivity/PWM5	04H	0101 0101	SEN_PWM_CH9				SEN_PWM_CH8			
Sensitivity/PWM6	05H	0101 0101	SEN_PWM_CH11				SEN_PWM_CH10			
Sensitivity/PWM7	06H	0101 0101	SEN_PWM_CH13				SEN_PWM_CH12			
Sensitivity/PWM8	07H	0101 0101	SEN_PWM_CH15				SEN_PWM_CH14			
Sensitivity/PWM9	08H	0101 0101	SEN_PWM_CH17				SEN_PWM_CH16			
Sensitivity/PWM10	09H	0101 0101	SEN_PWM_CH19				SEN_PWM_CH18			
Sensitivity/PWM11	0AH	0000 0101	–				SEN_PWM_CH20			
CTRL1	0BH	0100 1010	–	SSC	MS	FTC		RTC		
CTRL2	0CH	0001 0010	VPM	0	S/M_SEL	IMP_SEL	SRST	SLEEP	RB SEL	
Cal_Ctrl	0DH	1111 1010	BF_UP		BF_DOWN		BS_UP		BS_DOWN	
Port CTRL1	0EH	0000 0000	CH4		CH3		CH2		CH1	
Port CTRL2	0FH	0000 0000	–		CH7		CH6		CH5	
Port CTRL3	10H	0000 0000	CH11		CH10		CH9		CH8	
Port CTRL4	11H	0000 0000	CH15		CH14		CH13		CH12	
Port CTRL5	12H	0000 0000	CH19		CH18		CH17		CH16	
Port CTRL6	13H	0000 0000							CH20	
Cal_Hold1	14H	0000 0000	CH7	CH6	CH5	CH4	CH3	CH2	CH1	Dummy
Cal_Hold2	15H	0000 0000	CH14	CH13	CH12	CH11	CH10	CH9	CH8	–
Cal_Hold3	16H	0000 0000			CH20	CH19	CH18	CH17	CH16	CH15
Err_Percent	17H	0000 1101	–			Error Count			Error Percent	

TS20 (20-CH Auto Sensitivity Calibration Capacitive Touch Sensor)

Name	Addr. (Hex)	Reset Value (Bin)	Register Function and Description							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Output1	20H	0000 0000	-	CH7	CH6	CH5	CH4	CH3	CH2	CH1
Output2	21H	0000 0000	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Output3	22H	0000 0000	-	-	D-Error	CH20	CH19	CH18	CH17	CH16
Ref_wr_H	23H				Reference(13 ~ 8)					
Ref_wr_L	24H		Reference(7 ~ 0)							
ref_wr_CH1	25H	0000 0000	CH6	CH5	CH4	CH3	CH2	CH1	Dummy	-
ref_wr_CH2	26H	0000 0000	CH13	CH12	CH11	CH10	CH9	CH8	-	CH7
ref_wr_CH3	27H	0000 0000	CTRL	CH20	CH19	CH18	CH17	CH16	CH15	CH14
Sensitivity_rd_ctrl	28H	0000 0000	-			Read Channel Select				
Sensitivity_RD	29H		Sensitivity(7 ~ 0)							
Rd_CH	30H	0000 0000	CH6	CH5	CH4	CH3	CH2	CH1	Dummy	CTRL
Rd_CH	31H	0000 0000	CH13	CH12	CH11	CH10	CH9	CH8	-	CH7
Rd_CH	32H	0000 0000	-	CH20	CH19	CH18	CH17	CH16	CH15	CH14
Sen_H	33H		-	-	Sense(13 ~8)					
Sen_L	34H		Sense(7 ~ 0)							
Ref_H	35H		-	-	Reference(13 ~ 8)					
Ref_L	36H		Reference(7 ~ 0)							
Rd_CH	37H	0000 0000	CH6	CH5	CH4	CH3	CH2	CH1	Dummy	-
Rd_CH	38H	0000 0000	CH13	CH12	CH11	CH10	CH9	CH8	-	CH7
Rd_CH	39H	0000 0000	-	CH20	CH19	CH18	CH17	CH16	CH15	CH14

8.2 Sensitivity Control Register

Sensitivity / PWM x — Channel sensitivity and LED Dimming Control

Address (hex) : 00h ~ 0Ah

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	Sensitivity/PWM1	SEN_PWM_CH2[3:0]				SEN_PWM_CH1[3:0]			
01h	Sensitivity/PWM2	SEN_PWM_CH4[3:0]				SEN_PWM_CH3[3:0]			
02h	Sensitivity/PWM3	SEN_PWM_CH6[3:0]				SEN_PWM_CH5[3:0]			
03h	Sensitivity/PWM4	-				SEN_PWM_CH7[3:0]			
04h	Sensitivity/PWM5	SEN_PWM_CH9[3:0]				SEN_PWM_CH8[3:0]			
05h	Sensitivity/PWM6	SEN_PWM_CH11[3:0]				SEN_PWM_CH10[3:0]			
06h	Sensitivity/PWM7	SEN_PWM_CH13[3:0]				SEN_PWM_CH12[3:0]			
07h	Sensitivity/PWM8	SEN_PWM_CH15[3:0]				SEN_PWM_CH14[3:0]			
08h	Sensitivity/PWM9	SEN_PWM_CH17[3:0]				SEN_PWM_CH16[3:0]			
09h	Sensitivity/PWM10	SEN_PWM_CH19[3:0]				SEN_PWM_CH18[3:0]			
0Ah	Sensitivity/PWM11	-				SEN_PWM_CH20[3:0]			

Description

The sensitivity of channel is possible to adjust by Sensitivity/PWMx register. The following table shows detail information of sensitivity.

Bit name	Reset	Function	
SEN_PWM_CHx[3:0]	0101	Port Control bits of Port_CTRLx[3] are "00"	Sensitivity T (= thickness of PC) of Channels @ Cs = 0pF, Normal Step Sensitivity (SSC bit of CTRL1[4] Register is '1') 0000 : approximate sensor 0001 : 6.00 ~ 8.00 T 0010 : 4.50 ~ 6.00 T 0011 : 3.50 ~ 5.00 T 0100 : 3.50 ~ 5.00 T 0101 : 3.00 ~ 4.50 T 0110 : 2.25 ~ 3.50 T 0111 : 1.80 ~ 3.00 T 1000 : 1.40 ~ 2.50 T 1001 : 1.20 ~ 2.25 T 1010 : 1.00 ~ 2.00 T 1011 : 1.00 ~ 1.80 T 1100 : 0.75 ~ 1.50 T 1101 : 0.50 ~ 1.25 T 1110 : 0.50 ~ 1.00 T 1111 : 0.25 ~ 0.75 T
			Sensitivity T (= thickness of PC) of Channels @Cs = 0pF, Fine Step Sensitivity (SSC bit of CTRL1 Register is '0') 0000 : approximate sensor 0001 : approximate sensor 0010 : approximate sensor 0011 : 6.00 ~ 8.00 T 0100 : 5.50 ~ 7.00 T 0101 : 5.00 ~ 6.50 T 0110 : 4.50 ~ 6.00 T 0111 : 4.00 ~ 5.50 T 1000 : 4.00 ~ 5.00 T 1001 : 3.50 ~ 5.00 T 1010 : 3.00 ~ 4.50 T 1011 : 2.75 ~ 4.00 T 1100 : 2.50 ~ 3.75 T 1101 : 2.25 ~ 3.50 T 1110 : 2.00 ~ 3.25 T 1111 : 1.80 ~ 3.00 T
		"10"	LED dimming controllable up to 16 steps. 0000 : The minimum luminance(Almost Off) 1111 : The maximum luminance

[3] Refer to chapter 8.6 Port Control Register

[4] Refer to chapter 8.3 General Control Register 1

8.3 General Control Register 1

CTRL1 General Control Register1

Address (hex): 0Bh

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	SSC	MS	FTC[1:0]		RTC[2:0]		

Description

The calibration speed just after power on reset is very high during the time which is defined by FTC[1:0] to have a good adoption against unstable external environment.

Bit name	Reset	Function
RTC[2:0]	010	Response Time Control - Response period = RTC[2:0] + 2
FTC[1:0]	01	First Touch Control - 00 : 2.5 sec - 01 : 5 sec - 10 : 10 sec - 11 : 20 sec
MS	0	Operation Mode Selection - 0 : auto alternate (fast/slow) mode - 1 : fast mode
SSC	1	Sensitivity Step Control - 0 : Fine steps - 1 : Normal steps

8.4 General Control Register2

CTRL2 General Control Register 2

Address (hex): 0Ch

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
VPM	0	S/M_SEL	IMP_SEL	SRST	SLEEP	RB_SEL	

Description

If SRST bit is set by '1', digital block is reset except analog and I^2C block.

The SLEEP function allows getting very low current consumption when it is set.

It is possible to reduce the period of sensing burst if VPM bit is set. When user makes CS tact switch input or LED drive or channel hold, the period of sensing burst is calculated without that CS channel. And Bit6 must be zero.

Bit name	Reset	Function
RB_SEL	10	Internal System Frequency Speed Control - 00,01 : Fast - 10 : Normal - 11 : Slow
SLEEP	0	Sleep Mode Enable - 0 : Disable Sleep Mode - 1 : Enable Sleep Mode
SRST	0	Software Reset - 0 : Disable Software Reset - 1 : Enable Software Reset
IMP_SEL	1	Impedance Select - 0 : Low Impedance - 1 : High Impedance
S/M_SEL	0	Single/Multi Output Mode Select - 0 : Multi Mode - 1 : Single Mode
VPM	0	Variable Period Mode[5] - 0 : Disable - 1 : Enable

[5] Refer to Chapter 8.6 Port Control Register

8.5 Calibration Speed Control Register

Cal_ctrl Calibration Speed Control Register

Address (hex): 0Dh

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BF_UP		BF_DOWN		BS_UP		BS_DOWN	

Description

The calibration speed might be controlled on each operation mode by Cal_ctrl register.
If BS_DOWN is set "11", all calibration speed is followed this case(store reference register with sense count directly) and other register settings are ignored.

Bit name	Reset	Function
BS_DOWN[1:0]	10	Calibration speed control lower direction in BS mode - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Store reference register with sense count directly
BS_UP[1:0]	10	Calibration speed control upper direction in BS mode - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Slow
BF_DOWN[1:0]	11	Calibration speed control lower direction in BF mode - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Slow
BF_UP[1:0]	11	Calibration speed control upper direction in BF mode - 00 : Fastest - 01 : Fast - 10 : Normal - 11 : Slow

8.6 Ports Control Register

Port_ctrlx — Port Control Register

Address (hex): 0Eh ~ 13h

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Eh	PORT_CTRL1	CH4		CH3		CH2		CH1	
0Fh	PORT_CTRL2	-		CH7		CH6		CH5	
10h	PORT_CTRL3	CH11		CH10		CH9		CH8	
11h	PORT_CTRL4	CH15		CH14		CH13		CH12	
12h	PORT_CTRL5	CH19		CH18		CH17		CH16	
13h	PORT_CTRL6	-		-		-		CH20	

Description

CS1 ~ CS20 ports have a specific operation with Port_ctrlx register. The following table shows the detail information about specific operation.

Channel Hold operation is no working mode in specific channel.

And it is recommended to apply software reset when a port goes from other modes to sense.

Bit name	Reset	Function
CHx	00	Port Operation - 00 : Sense - 01 : Channel Hold - 10 : LED driver - 11 : Tact switch input

8.7 Channel Calibration Control Register

Cal_holdx — Dummy, Channel 1 ~ 7 Calibration Enable Register

Address (hex): 14h ~ 16h

Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
14h	Cal_Hold1	CH7	CH6	CH5	CH4	CH3	CH2	CH1	Dummy
15h	Cal_Hold2	CH14	CH13	CH12	CH11	CH10	CH9	CH8	-
16h	Cal_Hold3			CH20	CH19	CH18	CH17	CH16	CH15

Description

The calibration of each channel is independently available to control. Each channel is working even if a bit is set.

Bit name	Reset	Function
Dummy, Chx	0	Calibration Enable Control - 0 : Enable reference calibration (sensing + calibration) - 1 : Disable reference calibration (sensing + No calibration)

8.8 Noise Environment Overcome Control Register

Err_CTRL — Error mode entering / escape control

Address (hex): 17h

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
–	–	–	Err_Count			Err_Percent	

Description

Err_Percent bits are set by I2C interface. And this bit can control the detective noise level and count. It is possible to prevent malfunction by rapid changes of environment.

Bit name	Reset	Function
Err_Percent	01	Error detective level decision - 00 : 0.3% - 01 : 0.4% - 10 : 0.5% - 11 : 0.7%
Err_Count	011	Error detective count decision - 000 ~ 111 : [Err_Count] + 1

8.9 Output Register

Output1x — Channel Output Register

Address (hex): 20h ~ 22h

Type: R

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
20h	Output1	–	CH7	CH6	CH5	CH4	CH3	CH2	CH1
21h	Output2	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
22h	Output3			ND	CH20	CH19	CH18	CH17	CH16

Description

The each channel output of TS20 is provided with 1 bit. It represents to detect result as below table.

Bit name	Reset	Function
CHx	0	Output of channel x - 0: No touch - 1: Detected touch
ND	0	Noise Detect Indication - 0: Normal State - 1: Noisy State

8.10 Write Reference Count Register

Ref_count_H, Ref_count_L — Register to write the reference count

Address (hex) : 23h ~ 24h
Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
23h	Output1	x	x	Ref_count_H					
24h	Output2	Ref_count_L							

Description

User can write the reference data directly. And this register is the reference data register to write. If the channel user want to write and CTRL bit is set, reference data is updated with data user want.

Bit name	Reset	Function
Ref_count_H	xx000000	Reference Count high Byte[13 : 8]
Ref_count_L	00000000	Reference Count low Byte[7 : 0]

ref_wr_chx — Channel Register to write reference count

Address (hex): 25h ~ 27h
Type: R/W

Address	Register Name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
25h	ref_wr_ch1	CH6	CH5	CH4	CH3	CH2	CH1	Dummy	–
26h	ref_wr_ch2	CH13	CH12	CH11	CH10	CH9	CH8	–	CH7
27h	ref_wr_ch3	CTRL	CH20	CH19	CH18	CH17	CH16	CH15	CH14

Description

The channel register to write the reference data. And the selected channel reference data is updated at CTRL is to be high.

Bit name	Reset	Function
Dummy, CHx	0	Channel information - 0 : No select - 1 : Select.
CTRL	0	The Command bit to write reference data - 1 : Write the reference data (if CTRL bit is '1', user can not write the reference data) - 0 : wait until next command

8.11 Sensitivity Read

sen_rd_channel

Channel selection register to read sensitivity

Address (hex): 28h

Type: R/W

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
–	–	–	sen_rd_channel				

Description

It is possible to read the sensitivity of specific channel directly by I2C interface. And it is possible to select channel that user want to read the sensitivity by controlling sen_rd_channel register. The detail information is in following table.

Bit name	Reset	Function
sen_rd_channel	00000	The setting value of each channels - 00001 : Channel 1 - 00010 : Channel 2 - 00011 : Channel 3 - 00100 : Channel 4 - 00101 : Channel 5 - 00110 : Channel 6 - 00111 : Channel 7 - 01000 : – - 01001 : Channel 8 - 01010 : Channel 9 . . . . . - 10100 : Channel 19 - 10101 : Channel 20

Sensitivity_RD

The sensitivity data register to read

Address (hex): 29h

Type: R

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
sen_data							

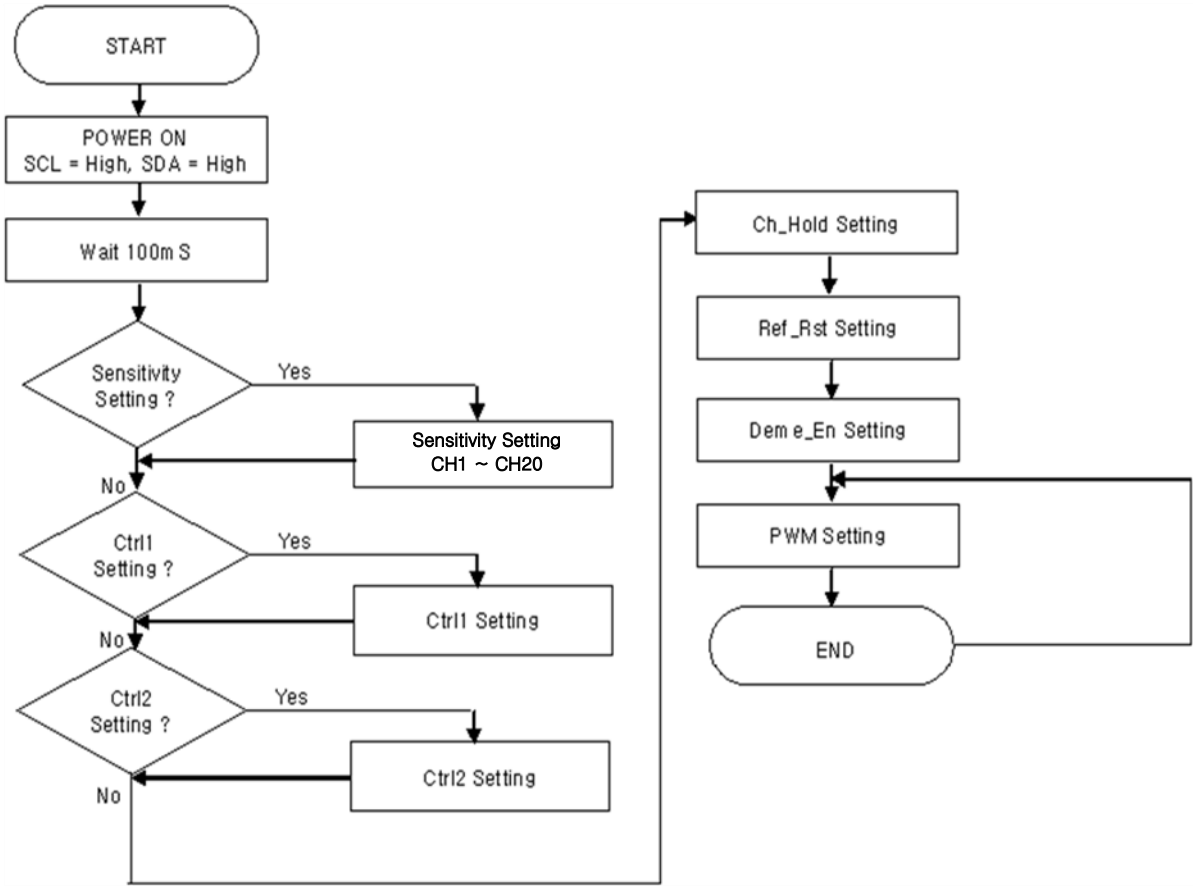
Description

It is possible to read the sensitivity of specific channel directly by I2C interface.

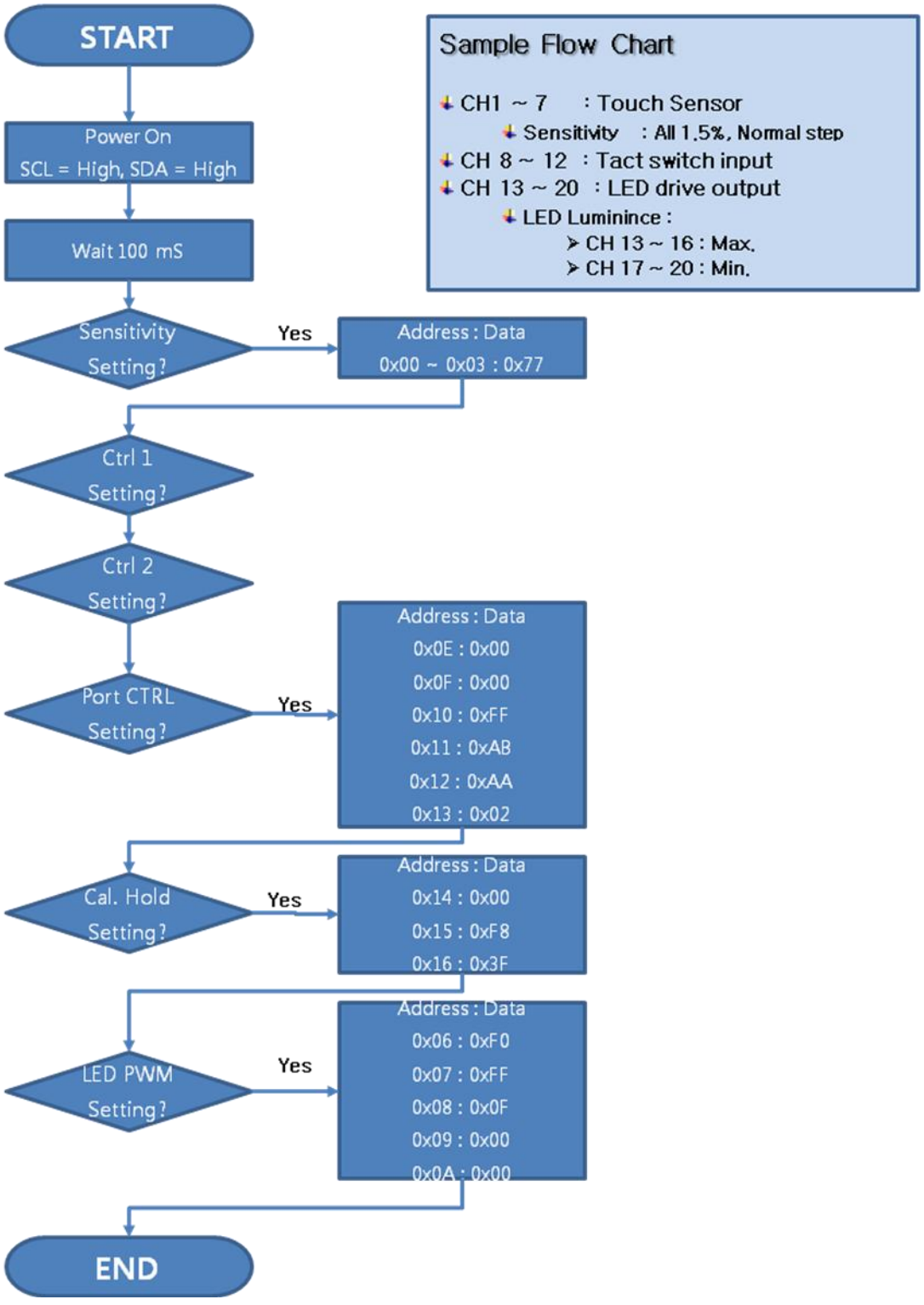
Bit name	Reset	Function
sen_data	00000000	The sensitivity data of selected channel - % = value / 2048

9 Recommended TS20 Power Up Sequence (Example)

9.1 Recommended TS20 Power Up Flow Chart

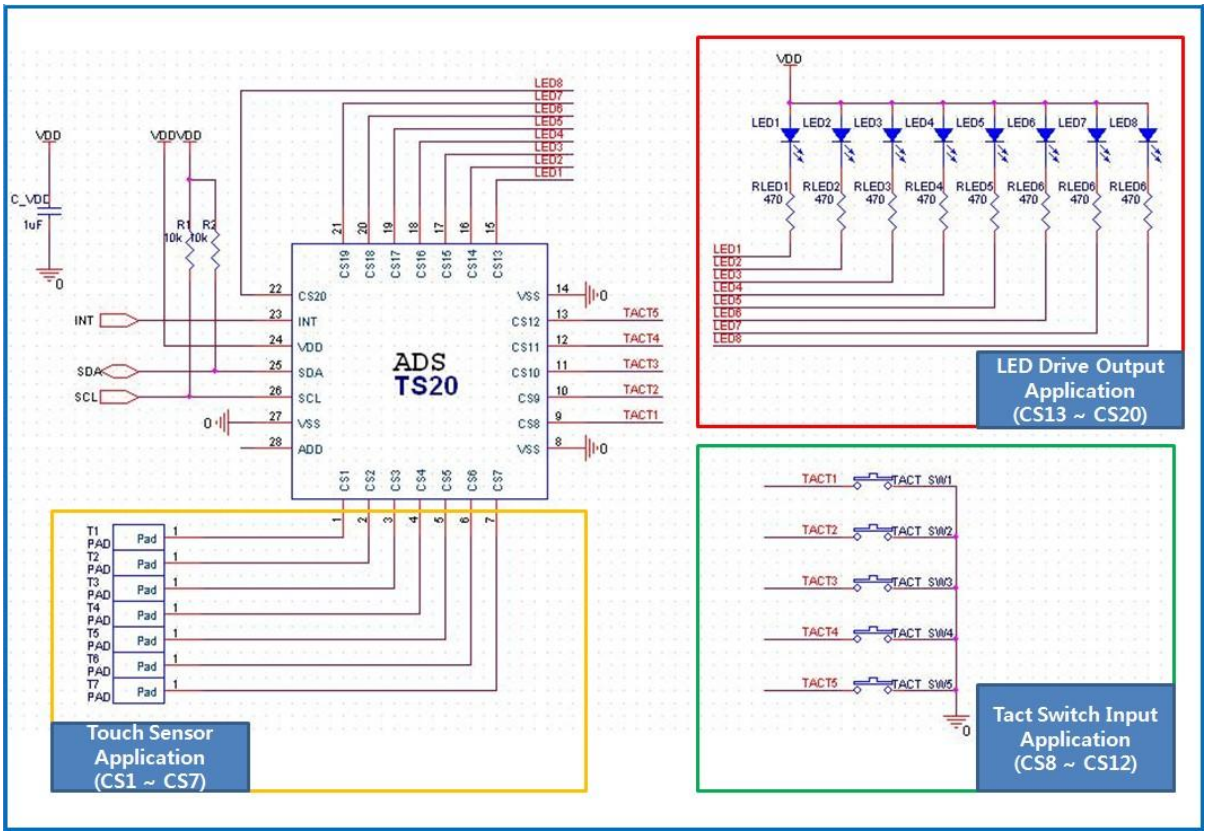


9.2 Recommended TS20 Power Up Sequence Sample



10 Recommended Circuit Diagram

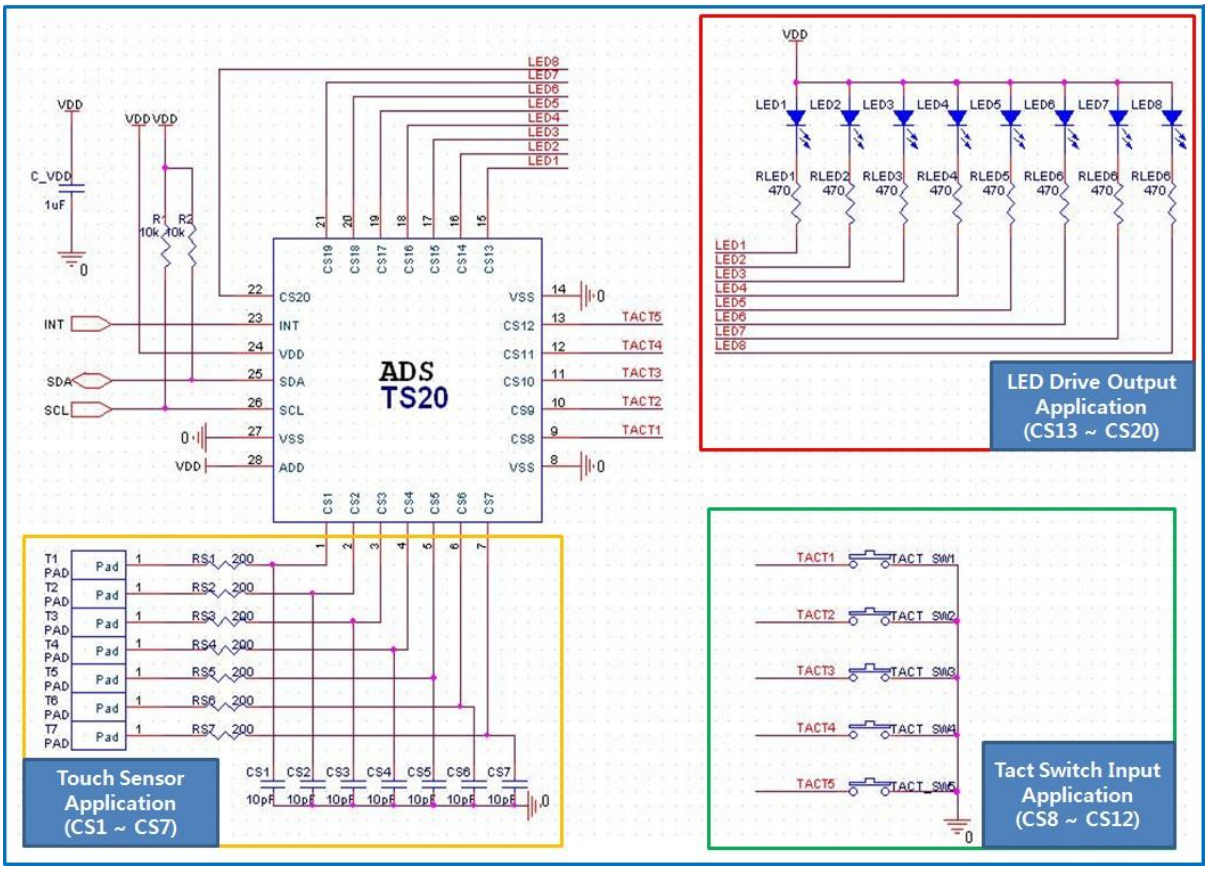
10.1 Application Example in clean power environment



TS20 Application Example Circuit (Clean power environment)

- The CS patterns also should be routed as short as possible and the width of line might be about 0.25mm (or narrower line).
- The capacitor that is between VDD and GND is an obligation. It should be located as close as possible from TS20.
- The CS pattern routing should be formed by bottom metal (opposite metal of touch PAD).
- The empty space of PCB must be filled with GND pattern to strengthen GND pattern and to prevent external noise from interfere with sensing frequency.
- The TS20 is reset when power rise from 0V to proper VDD
- The LED_GND and GND should be short in the system and the lines are recommended to be split from the most low impedance ground point to avoid ground bouncing problems.

10.2 Application Example in noisy environment

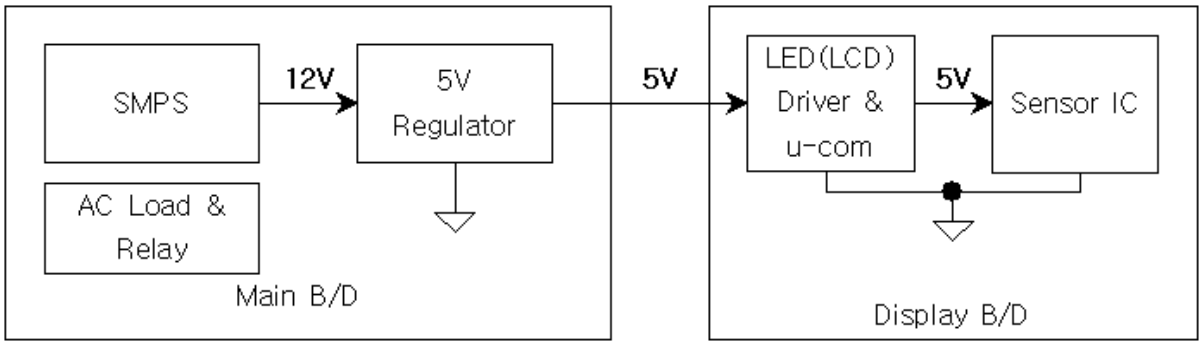


TS20 Application Example Circuit (Noisy environment)

- The VDD periodic voltage ripple over 50mV and the ripple frequency is lower than 10 kHz can cause wrong sensitivity calibration. To prevent above problem, power (VDD, GND) line of touch circuit should be separated from other circuit. Especially LED driver power line or digital switching circuit power line certainly should be treated to be separated from touch circuit.
- Thanks to the RS1 ~ RS20, CS1 ~ CS20 and CS20, the noise immunity could be improved.
- The LED_GND and GND should be short in the system and the lines are recommended to be split from the most low impedance ground point to avoid ground bouncing problems.

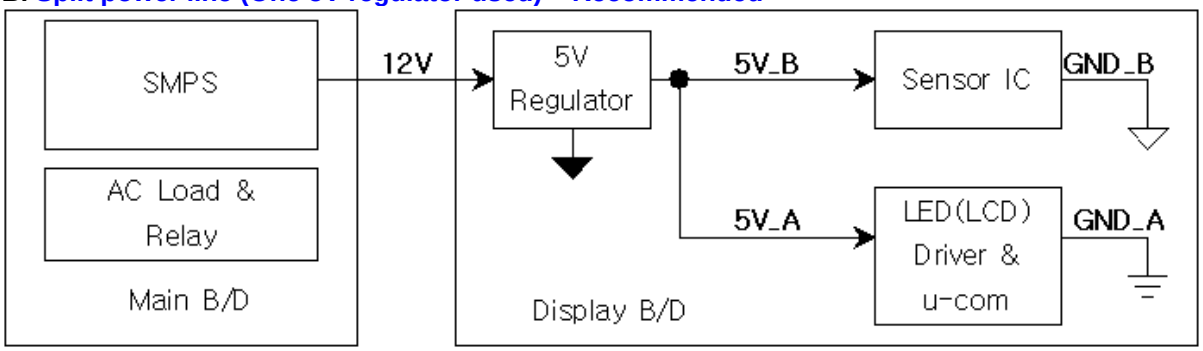
10.3 Example – Power Line Split Strategy PCB Layout

A. Not split power line (Bad power line design)

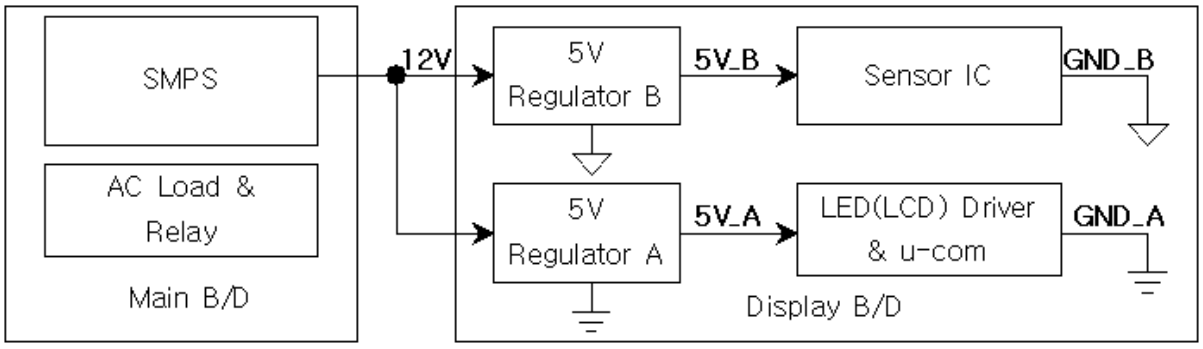


- The noise that is generated by AC load or relay can be loaded at 5V power line.
- A big inductance might be appeared in case of the connection line between main board and display board is too long, moreover the voltage ripple could be generated by LED (LCD) display driver at VDD (5V).

B. Split power line (One 5V regulator used) – Recommended

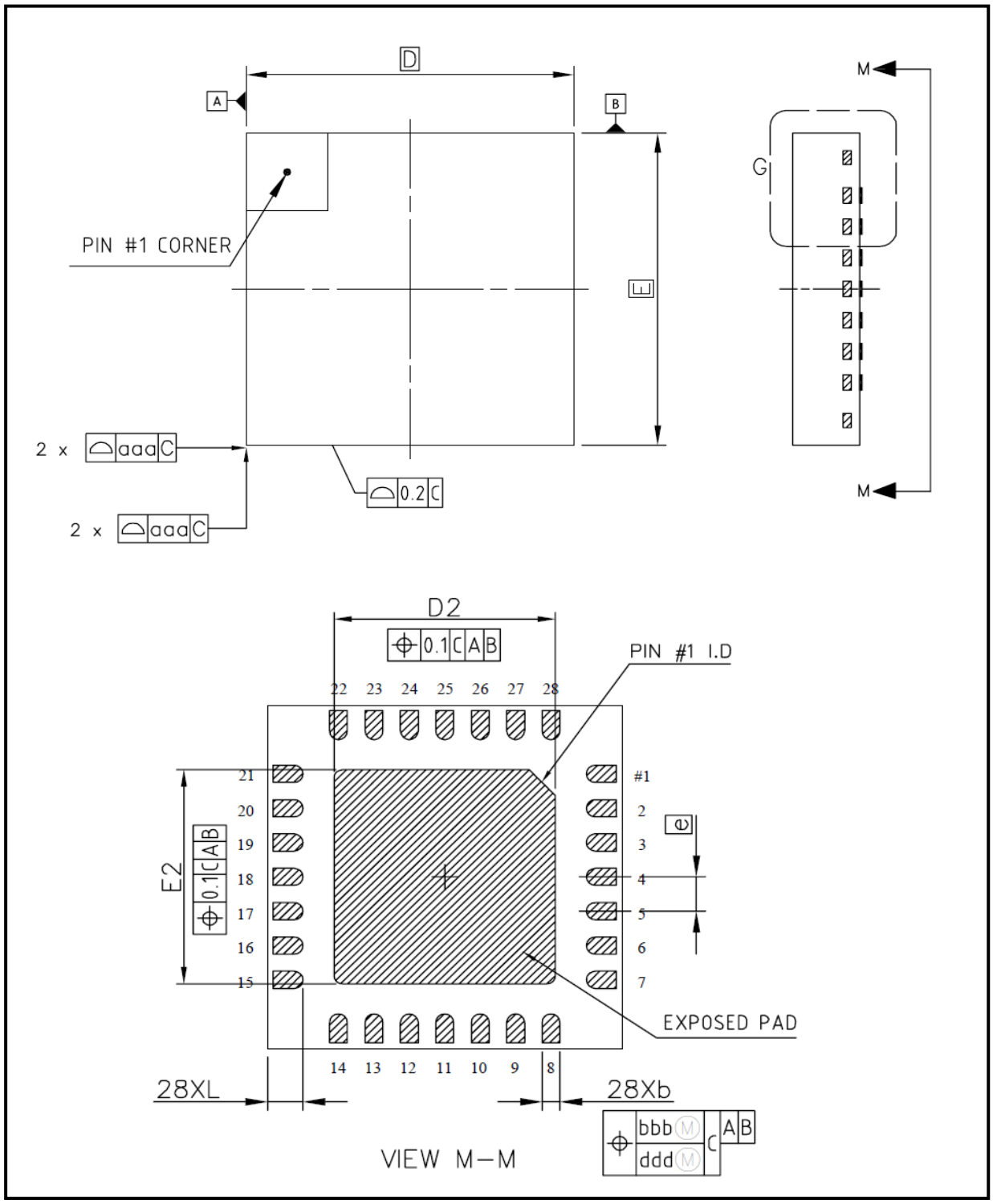


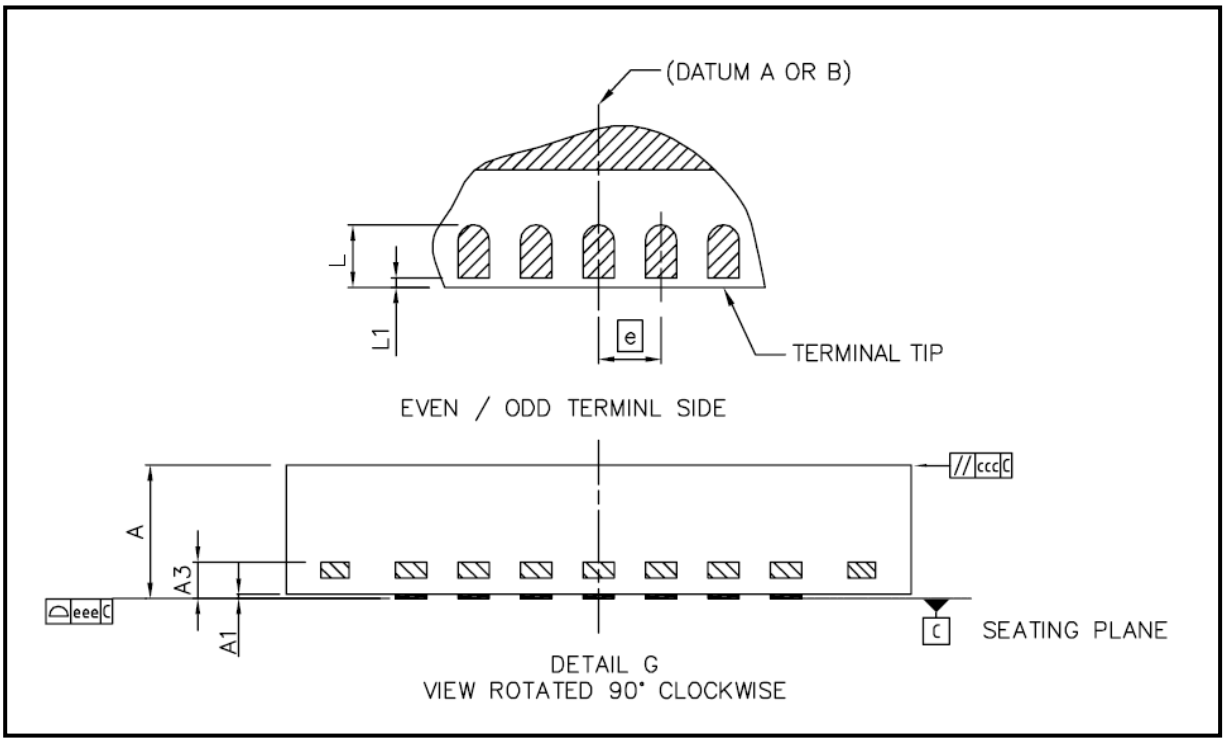
C. Split power line (Separated 5V regulator used) – Strongly recommended



11 MECHANICAL DRAWING

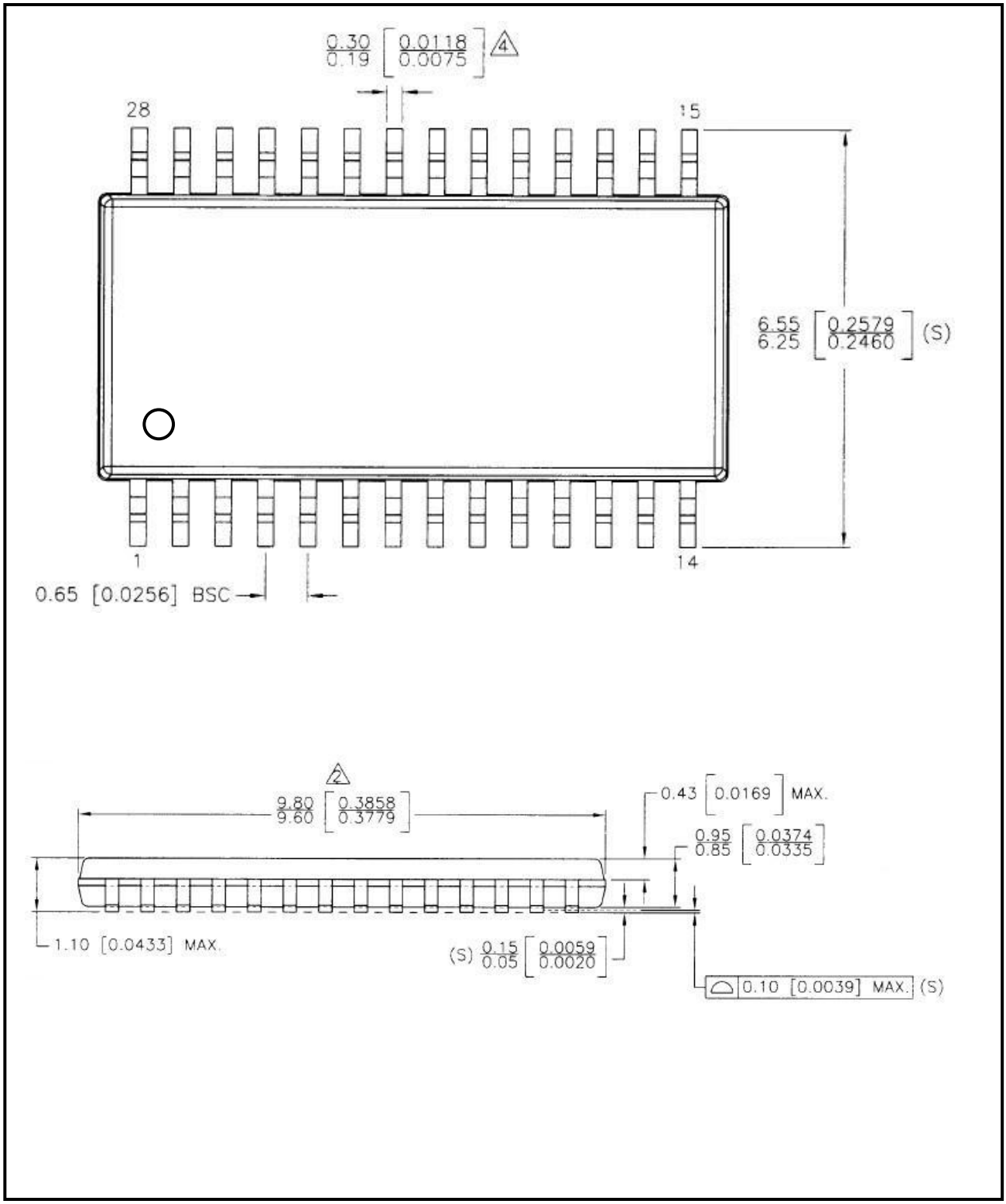
11.1 Mechanical Drawing of TS20 (28 QFN)

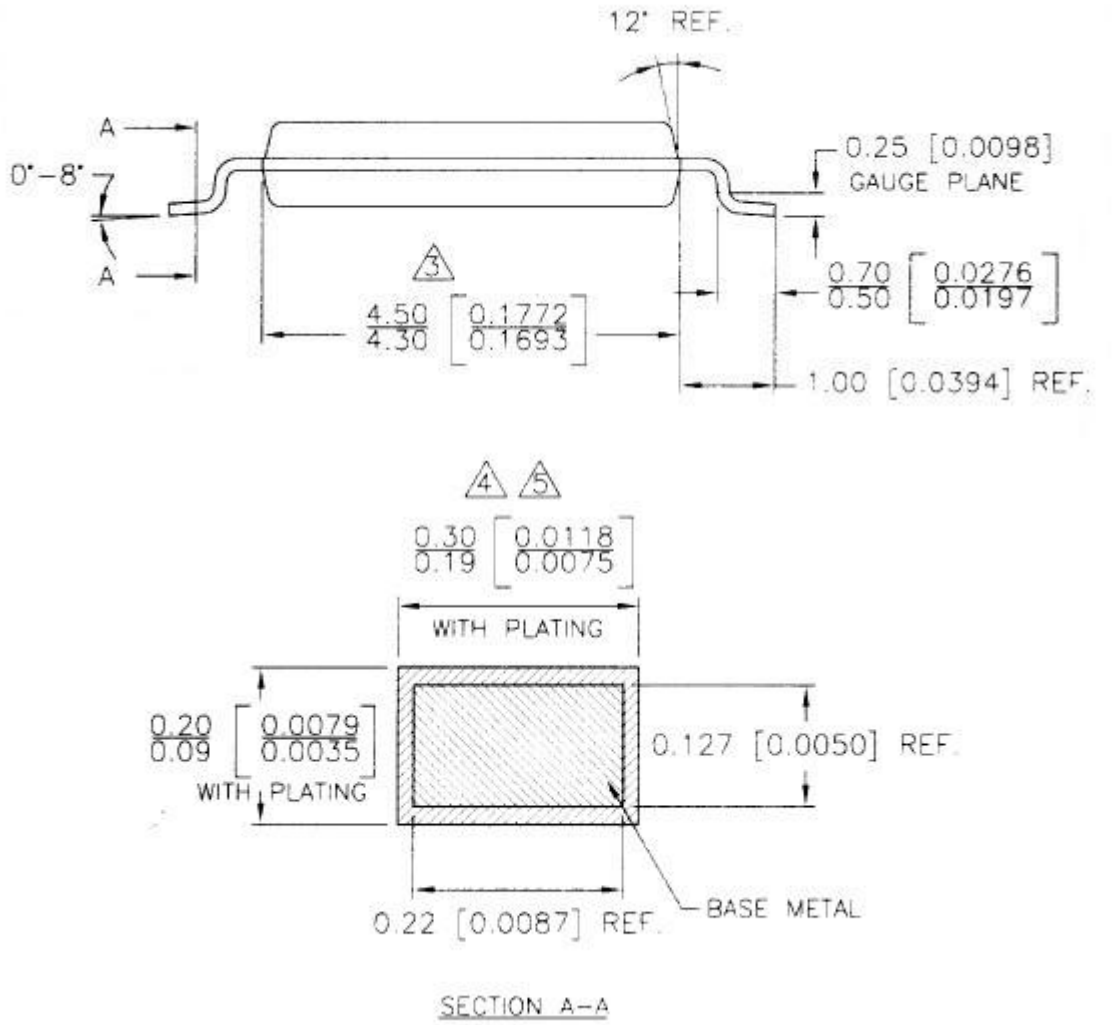




DIM	MIN	NOM	MAX	NOTES
A	0.80	0.85	0.90	1.0 DIMENSIONING & TOLERANCEING CONFIRM TO ASME Y14.5M-1994
A1	0.00		0.05	
A3		0.203 REF		
b	0.15	0.20	0.25	2.0 ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
D		4.00 BSC		
E		4.00 BSC		
e		0.40 BSC		3.0 DIMESION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP. DIMENSION L1 REPRESENTS TERMINAL FULL BACK FROM PACKAGE EDGE UP TO 0.1mm IS ACCEPTABLE.
D2	2.40	2.50	2.60	
E2	2.40	2.50	2.60	
L	0.35	0.40	0.45	
L1	0.00		0.10	
aaa		0.10		4.0 COPLANARITY APPLIES TO THE EXPOSED HEAT SLUG AS WELL AS THE TERMINAL.
bbb		0.10		
ccc		0.10		
ddd		0.05		5.0 RADUS ON TERMINAL IS OPTIONAL.
eee		0.08		

11.2 Mechanical Drawing of TS20 (28 TSSOP)





SECTION A–A

NOTE :

1. CONTROLLING DIMENSIONS IN mm. [Inches.]
2. DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm. PER SIDE.
3. DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm.PER SIDE.
4. DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM.
5. CROSS SECTION A–A TO BE DETERMINED AT 0.10 TO 0.25 MM. FROM LEAD TIP.
6. LEAD SPAN / STAND OFF HEIGHT / COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERSITIC.(S)
7. THIS PART COMPLIANT WITH JEDEC SPECFICATION MO–153 VARIATION AE.

12 MARKING DESCRIPTION

Device Code : **T S 2 0**

- **Channel Number**
- **Touch Switch Group**

Weekly Code : **YY WW**

- **Manufacturing Week**
- **Manufacturing Year**

NOTES:

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